DAT

NEW TECHNICAL THEORY FOR SERVICING

TCD-D3

OPERATION MANUAL

DIGITAL AUDIO TAPE RECORDER

SONY®

1. Overview

The TCD-D3 is one of the world's smallest and lightest portable DATs that incorporate an A/D converter. Based on the Serial Copy Management System (SCMS), it allows direct recording of digital signals from compact discs, provides up to four continuous hours of recording in the LP mode, and comes with numerous other features. In addition, its mechanical deck section is comprised of densely-mounted, 4- layer circuit boards and incorporates a newly developed, 15mm-diameter head drum, resulting in greatly reduced weight and size.

1.1 Compact and Lightweight

Compared with 30mm-diameter head drums used in conventional models, the TCD-D3's mechanical deck section (or simply mecha deck) uses a newly developed 15mm-diameter head drum. This has brought about a great reduction in weight and size. In fact, the cubic volume and weight of the TCD-D3's mecha deck are both approximately 2/5 those of conventional models (345 cm^3 → 138 cm^3; 300 g → 125 g). Furthermore, the mecha deck uses densely-mounted, 4-layer circuit boards which are only 0.6 mm in overall thickness as shown in Figure 1-1.

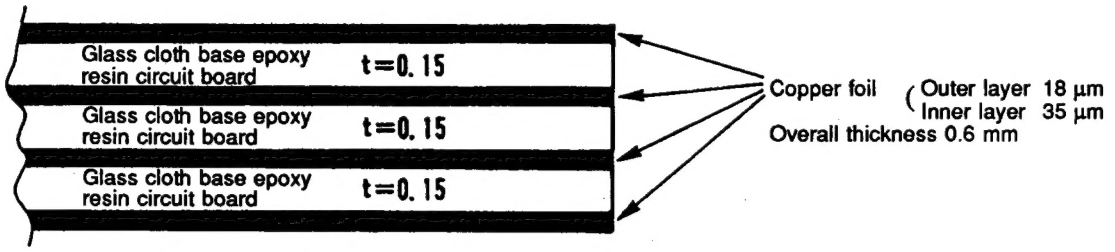


Figure 1-1. Structure of 4-Layer Circuit Board

1.2 Long-Hour Recording

Thanks to its second-generation LSI (CXD2601AQ), the TCD-D3 provides up to four continuous hours of recording with a single DT-120 tape when recorded in the 12-bit non-linear 32K LP mode (option 2) as shown in Table 1-1.

Table 1-1. Recording Modes and Examples of Input Sources

	Maximum recording time	Sampling frequency	Quantization bits	Typical inputs and sources
48K mode (standard)	120 min.	48kHz	16-bit linear	Digital (DAT, satellite broadcast B-mode)
				Analog (general sources)
32K mode (option 1)	120 min.	32kHz	16-bit linear	Digital (Satellite broadcast A-mode)
32K LP mode (option 2)	240 min.	32kHz	12-bit non-linear	Digital (Satellite broadcast A-mode)
				Analog (general sources)
44K mode	120 min.	44kHz	16-bit linear	Digital (CD)

* For digital inputs, the recording mode is automatically determined according to the digital signal sampling frequency. The 32kHz mode can be selected between options 1 and 2, however.
* For recording from analog inputs, the user can select the 48K or 32K LP modes regardless of the input source.

1.3 Other Features

- Using the auxiliary battery pack (BP-D3), the TCD-D3 provides approximately two hours of recording and reproduction after one hour of recharging.

- Incorporates a liquid crystal display backlighted by EL (electroluminescence) for easy legibility.

- Comes with a start ID write function which allows quick search at about 100 times normal speed.

- Allows fast cue/review (25 times normal speed) in addition to standard cue/review (3 times normal speed).

- Provides an indication of "absolute time" to show a cumulative time of recording from the beginning of tape.

- Provides an indication of "sampling frequency" to show the sampling frequency of the signal during recording and playback.

- Incorporates an auto power supply method for use with a separately available stereo microphone (ECM-S220).

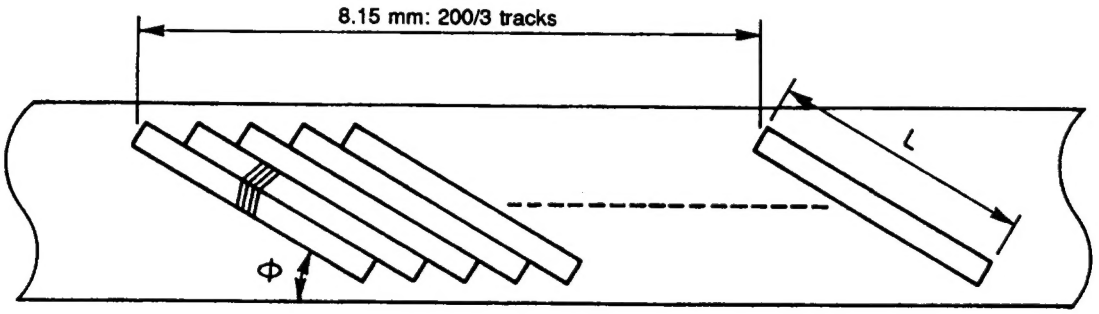
- Comes with a microphone attenuator (-20 dB) to suppress excessive inputs.

2. Recording Format

2.1 DAT Format

For the DAT format, the track patterns recorded on tape are defined as shown in Figure 2-1.

With conventional DATs using 30mm-diameter head drums, this track pattern is implemented by formulating specifications that the head drum speed is 2,000 rpm, the tape winding angle relative to the head drum is 90°, and that the helical-wound tape inclination relative to the head drum (still angle θ) is 6° 22' as shown in Figure 2-2. Table 2-1 shows the primary recording format specifications of 30mm drum diameters for your reference.



Tape speed (mm/sec)	8.15
Number of tracks per second	200/3
Track angle	6° 22' 59.5"
Track length (mm)	23.501
Track pitch (μm)	13.591

Figure 2-1. Recording Format in Standard Mode

Table 2-1. Primary Recording Format Specifications (Drum Diameter 30 mm)

Item \ Mode	Recording/playback mode				Playback-only mode
	(48K mode)	(32K mode)	(32K-LP mode)	(44K mode)	(44K-WT mode)
Number of channels (CH)	2	2	2	2	2
Sampling frequency (kHz)	48	32	32	44.1	44.1
Resolution of quantization (bit)	16 (linear)	16 (linear)	12 (non-linear)	16 (linear)	16 (linear)
Transmission rate (Mbps)	2.46	2.46	1.23	2.46	2.46
Subcode capacity (kbps)	273.1	273.1	136.5	273.1	273.1
Modulation method	8-10 modulation				
Error correction method	Duplex Reed Solomon code				
Tracking system	Area-divided ATF				
Cassette size (mm)	73 x 54 x 10.5				
Recording time (minute)	120	120	240	120	80
Tape width (mm)	3.81				
Type of tape	Metal powder				Oxide tape
Tape thickness (μm)	13 ± 1μ				
Tape speed (mm/s)	8.15	8.15	4.075	8.15	12.225
Track pitch (μm)	13.591				20.41
Track angle	6° 22'59.5"				6° 23'29.4"
Drum specification	ϕ30 90° lap				
Drum revolution (rpm)	2.000		1.000	2.000	2.000
Relative speed (ϕ = 30) (m/s)	3.133		1.567	3.133	3.129
Head azimuth angle	± 20°				

2.2 Compatibility with 30mm-Diameter Drums

To obtain the same track length as with 30mm-diameter head drums by using a 15mm-diameter head drum, the tape winding angle relative to the drum must be extended to 180° as shown in Figure 2-3 because its diameter is half that of the 30mm- diameter drum.

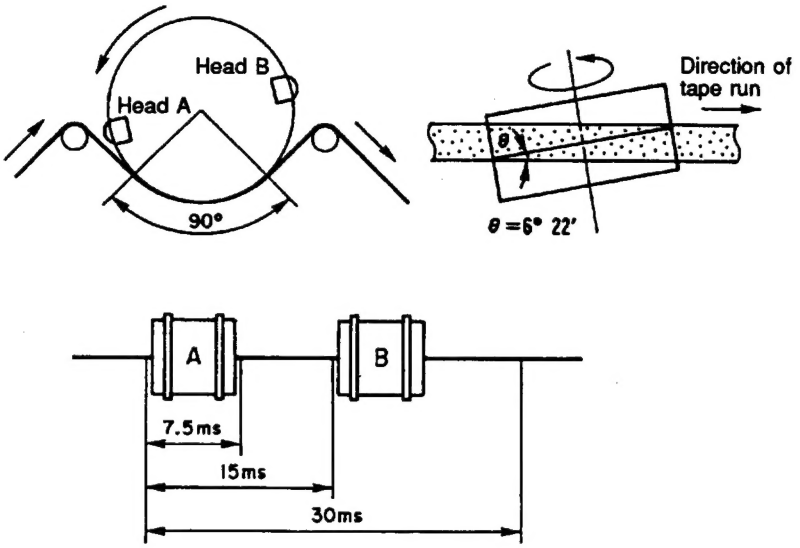


Figure 2-2. Track Length with 30mm-Diameter Drum

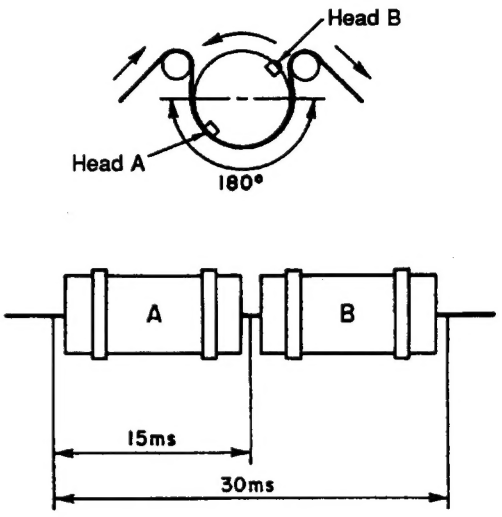


Figure 2-3. Track Length with 15mm-Diameter Drum

Concerning the head drum speed, a normally employed method is to double the speed of a 30mm-diameter drum to 4,000 rpm to obtain the same tape-to-head relative speed for a 15mm- diameter drum as with a 30mm-diameter drum. For the TCD-D3, however, a different method is employed so that the drum is driven at a speed of 2,000 rpm as in the case of a 30mm- diameter drum. Since the tape-to-head relative speed is halved, this method results in track angle ϕ (shown in Figure 2-4) becoming larger than that of a 30mm-diameter drum and is therefore unable to obtain a format-designated track angle by using the same still angle as with a 30mm- diameter drum. To solve this problem, the mecha deck of the TCD-D3 has had its still angle θ reduced by approximately 1' than that of a 30mm-diameter drum.

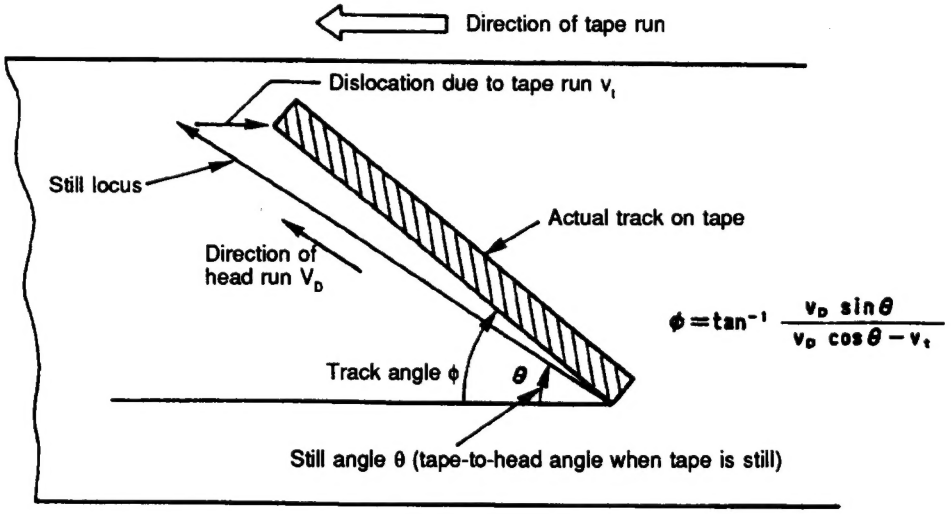


Figure 2-4. Relationship between Track and Still Angles

With this method, the signal waveform is such that the blank sections are filled by extending the waveform of a 30mm- diameter drum twice as much in the time-base direction as shown in Figure 2-3, resulting in the signal transmission rate being halved. Although this requires a modification of the timing to read data from tape, once the read data is arranged in memory, the rest is only to send that data to the D/A converter sequentially, same as in the case of a 30mm- diameter drum.

Thus, as explained above, the mecha deck using the 15mm- diameter drum provides compatibility with 30mm-diameter drums.

3. System Configuration

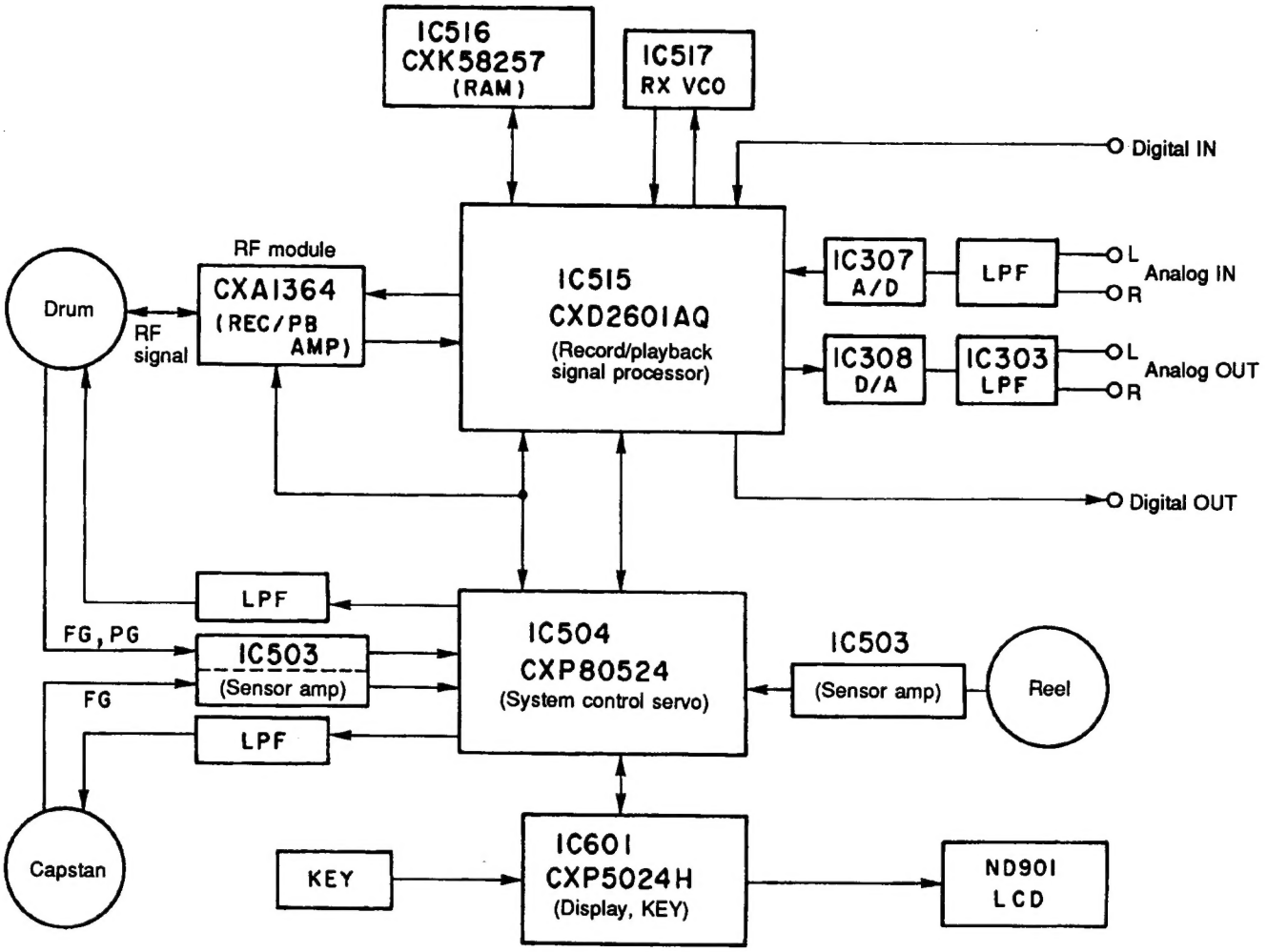


Figure 3-1. General System Configuration

The entire system of the TCD-D3 is configured around two primary processors: second-generation LSI (CXD2601AQ) as the signal processing block and the CXP80524 as the system control servo block as shown in Figure 3-1. The CXD2601AQ contains all the digital signal processing circuits required for recording and playback plus a digital I/O signal processing circuit and a non-tracking (NT) demodulation processing circuit used for reproduction in the LP mode. The A/D converter used in this block is a 64-fold oversampling 1-bit type incorporating a digital filter and the D/A converter is an 8-fold oversampling 18-bit ladder resistor type. The CXP80524 consists of servo circuits to control each of the drum, capstan, and reel servos via software, in addition to the basic function to control the operation of the entire system. Other noteworthy circuits are the CXP5024 used for KEY input detection, which incorporates a LCD controller/driver and the CXA1418N used to reshape the reel FG, capstan FG, and drum FG and PG waveforms, which integrates these functions into a single chip.

4. Description of Circuit Operation (See Block Diagram)

4.1 Signal Processing Block

4.1.1 Operation during Recording

The analog signal from the MIC/LINE IN terminal is input to the A/D converter via the microphone and line amps.

This signal is converted into 16-bit digital signal as it is 64-fold oversampled by the A/D converter (IC307) of a 1-bit quaternary delta-sigma modulation type, and is stripped of loop-back noise through filtration arithmetic operation by the built-in digital filter. Because the A/D converter performs high-order oversampling, the low-pass filter in the preceding stage is greatly simplified. The resulting 16-bit PCM data is interleaved along with subcode data (i.e., absolute time, program number, ID) sent from the system control servo (IC504) and appended with C1 and C2 parities in the signal processor (IC515) and RAM (IC516), respectively. The signal is finally fed into the RF module after being subjected to 8-10 modulation and then appended with an ATF signal.

Although two 64K-bit RAM chips capable of processing 2-track data were used in the DTC-1000ES and other first-generation models, the TCD-D3 uses RAM chips of twice the capacity of conventional ones, that is, 256K bits, to enable NT demodulation processing in the LP mode.

In the RF module, the recording data (REDT) from the signal processor (IC515) is amplified by a recording amp and then recorded on magnetic tape alternately by heads A and B at the timing pulsed by SWP.

4.1.2 Operation during Reproduction

The RF signal read from the rotary head is first amplified by a reproduction EQ circuit in the RF module. The reproduction signal (RFDT) component of this signal is presented to the signal processor (IC515) and the pilot crosstalk from adjacent tracks (ATF PILOT) separated from the main component in the RF module is fed into the system control servo (IC504).

In the signal processor (IC515), the signal is deinterleaved to and from RAM after being 10-8 demodulated in reverse order of recording. The signal is then detected and corrected of errors; if uncorrectable, the data is interpolated to correct errors. Then, the PCM data is output to the digital filter (IC302) and level meter/data generator (IC505). The subcode data is output to the system control servo (IC504) to display absolute time, program number, and other information, as well as control the system control circuit to, for example, locate the beginning of a selection by means of ID.

In the digital filter (IC302), the 16-bit PCM data which is input at a sampling rate of fs, is oversampled with 8fs and converted into 18-bit quantity.

The data is then stripped of sampling noise by digital filter computation. In addition to these, the digital filter also contains digital deemphasis and digital attenuator functions which are controlled by the system control servo (IC504). A D/A converter of multi-bit ladder resistor type (IC308) is used for digital-to-analog conversion. After being D/A converted, the 18-bit serial data from the digital filter (IC302) is output through a low-pass filter of third-order active type (IC303) to the headphone amp (IC304) and line out (J302).

Note that due to the way the system control servo (IC504) performs arithmetic operation, the level meter/data generator (IC505) divides 16-bit serial data into units of 4-bit parallel data and outputs them to the system control servo (IC504) for display on the level meter.

4.1.3 Operation during Digital Input/Output

The digital signal from digital audio equipment (e.g., CD player, BS tuner) input from the remote digital I/O terminal to the TCD-D3 circuit is input to the RX pin of the signal processor (IC515) after having its waveform reshaped.

This digital signal is based on the digital audio interface format and consists of a preamble, audio data, and control signal. It is serially transmitted left and right alternately with the preamble functioning as a sync signal.

The signal processor (IC515) generates a clock based on this preamble using the analog PLL (IC517) and takes in data with this clock timing. The separated audio data is presented to the digital signal processing block, and the emphasis, ID, and other control signals are output to the system control servo (IC504).

The digital signal is input to the internal circuit from the digital signal processing block for audio data, and from the system control servo (IC504) for control signals. It is then arranged of bits according to the digital audio interface format and subjected to modulation based on the biphase mark code rules in the signal processor (IC515) before being output from the TX pin.

4.2 Servo System

4.2.1 Drum Servo

The PG and FG outputs from the drum are input to the system control servo (IC504) after having their waveforms reshaped by a sensor amp.

The FG signal is first measured of the FG period and subtracted from the reference data in the system control servo (IC504). Servo calculation is made based on this deviation data, and the resulting error data is output as PWM signal with the fundamental frequency of 36.75 kHz. This provides control for speed servo.

In the meantime, the switching pulse (SWP) is generated from PG and FG in the system control servo (IC504). This SWP is phase-compared with drum reference (DREF) generated from the interleave reference signal, and the result is added to the speed error data as phase error data. The PWM output of the error data is converted into analog voltage by a low-pass filter and fed to the drum motor via a drive circuit. The motor revolution is thereby controlled so that the motor rotates at 2,000 rpm in the SP mode or 1,000 rpm in the LP mode during recording, and at 2,000 rpm during playback.

4.2.2 Capstan Servo

FG from the capstan motor is input to the system control servo (IC504) after having its waveform reshaped by a sensor amp as in the case of drum servo. The capstan servo during recording is measured of FG periods for respective speeds and subtracted from the reference data in the system control servo (IC504). Servo calculation is made based on this deviation data, and the resulting error data is output as PWM signal with the fundamental frequency of 36.75 kHz. After being converted into analog voltage by a low-pass filter, the data is applied to the capstan motor for speed control via a drive circuit so that the tape speed is maintained at 8.15 mm/s in the SP mode and 4.075 mm/s in the LP mode.

During playback, the system control servo (IC504) extracts ATF sync signals (522 kHz, 784 kHz) from the reproduction RF signal (RFDT) sent from the RF module and generates sampling pulses based on these sync signals.

In the meantime, the ATF pilot (130 kHz) envelope detection output (ATF PILOT) for crosstalk from the adjacent tracks are input from the RF module to the IC504. In this circuit, the peak values of the respective crosstalks are converted into 8-bit digital data, and the values sampled at the timing of the sampling pulses are subtracted from the data. The result is added to the capstan servo data as an ATF error after being multiplied by a value equivalent to the gain. The capstan motor is thereby controlled to ensure that the head traces tape tracks correctly.

During playback in the LP mode, the drum is driven at the same speed of 2,000 rpm as in the SP mode. Consequently, because the tape speed in the LP mode is half that of the SP mode, the head runs on tape at a different angle than in recording.

However, since the head reads the same track twice, audio reproduction data is generated selectively from either of the two, one which did not have any error after error correction. In the LP mode, therefore, ATF servo is applied to ensure that either of the twice-read reproduction data is read more correctly than the other.

4.2.3 Reel Servo

The takeup and supply reel bases are driven by the capstan motor via four relay gears.

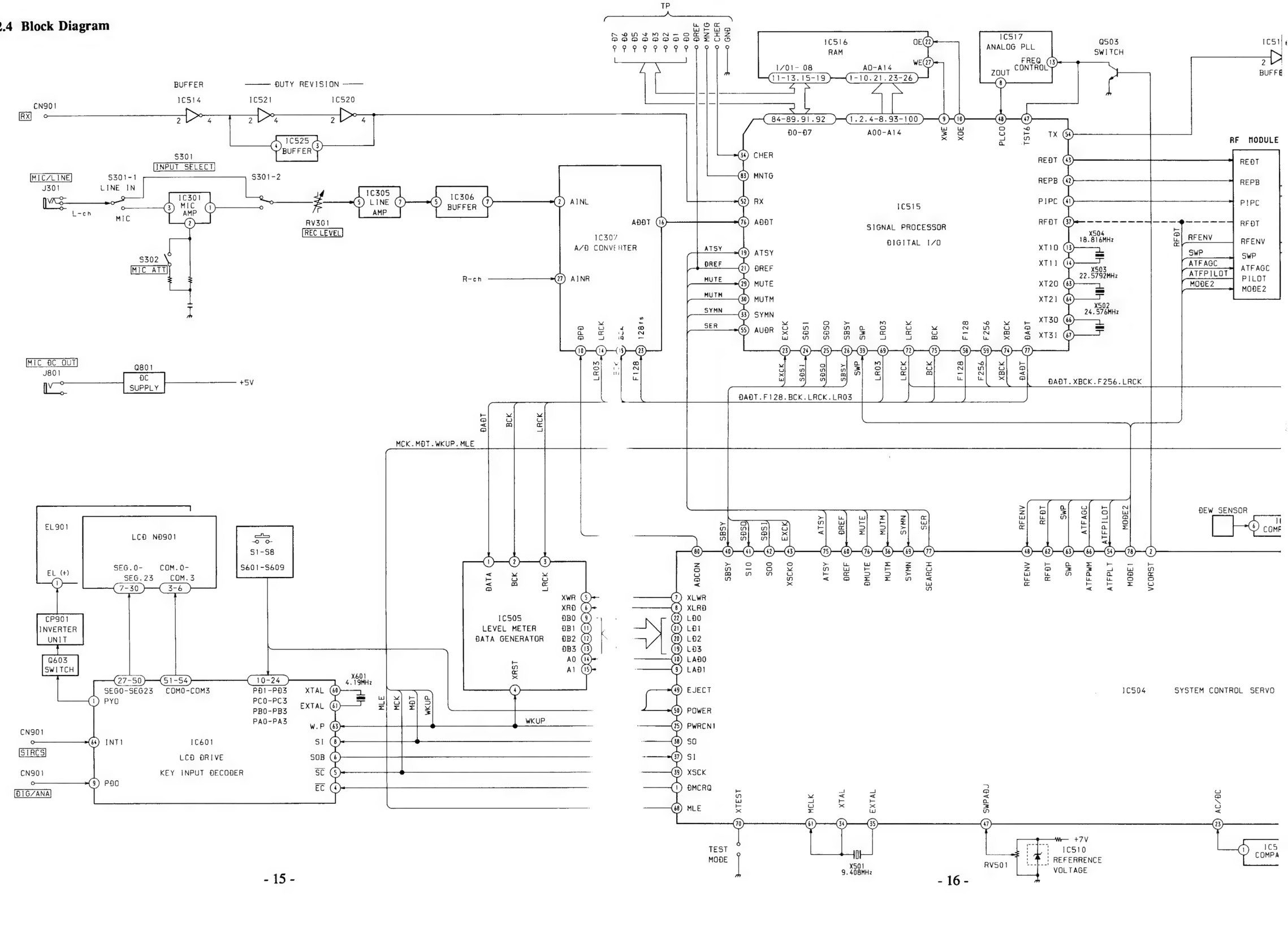
Reel servo is used when driving tape at high speed for search or FF/REW. To maintain constant tape speed regardless of the length of tape, reel servo is applied by controlling the capstan motor speed after calculating the current tape speed from the FG periods of both reels.

FG on both the takeup and supply reels are also used to indicate the linear counter and the remaining time of tape.

The duration required for one revolution of both reels is measured using a value obtained by integrating the duration of one FG period for 24 divisions, that is, one reel rotation, and is displayed on the linear counter after calculation.

For remaining time indication, the remaining time is calculated by processing the data on tape length (type), etc. obtained in the measure mode and the measured values of FGs of the two reels.

4.2.4 Block Diagram



IC519
BUFFER
CN901
RF MODULE
DRUM ASSY
REDT
REPB
P1PC
RFDT
RFENV
SWP
ATFAGC
PILOT
MODE2
DADT
DIGITAL FILTER
DIN
XTI
LRCI
BCKI
DOL
DOR
WCKO
BCKO
IC302
IC308
D/A CONVERTER
DATA(L)
DATA(R)
LEC
CLOCK
Vout(L)
Vout(R)
IC303
LPF
-7V
+5V
+7V
Q302
REG.
Q301
REG.
RV302
VOLUME
IC304
HEADPHONE
AMP
J303
PHONES
Q102
MUTE
J302
LINE OUT
L
Q303
MUTE
Q101
MUTE
Q507
MUTE
LMUTE
MDT
MCK
MLE
RST
WKUP
ROTARY
ENCODER
LOAD/UNLOAD
DET
REC PROOF
CASSETTE DET
CASSETTE CONTROL
LOCK
S1001
S1002
REI
REM
RED
RELD
REULD
RECINH
CASIN
CASLK
IC501
CAPSTAN MOTOR
DRIVE
CAPSTAN MOTOR
CAPPWM
XSTBY
XCAPON
CAPDIR
CAPFG
IC518
FILTER
Q502
BUFFER
STBY
CFG
IC503
SENSOR AMP
FG
IC502
DRUM MOTOR
DRIVE
DRUM MOTOR
DRMPWM
XDRMON
DRMPG
DRMFG
Q501
BUFFER
BREAK
DPG
DFG
PG AMP
FG AMP
PG
FG
IC503
SENSOR AMP
TRLFG
SRLFG
TR
SR
PH1002
T REEL SENSOR
PH1001
S REEL SENSOR
PLGON
Q505
PLUNGER DRIVE
PM1001
PLUNGER
IC511
MODE MOTOR
DRIVE
CTRMA
CTRMB
M1001
MODE MOTOR
(GEAR MOTOR)
CP501
DC-DC
CONVERTER
-7V
+7V
+5V
Vin
CONT
BATTERY PACK
(BP-03)
J501
DC IN 9V
Q1001
Q1002
IC513
END SENSOR
IC512
COMPARATOR
TEND
SEND
DEW SENSOR
IC509
COMPARATOR
STEM CONTROL SERVO
AC/DC
BATTERY
PWRCND
IC506
REG

5. Power Supply Circuit

Figure 5-2 shows a block diagram of the power supply circuit.

The power supplied from the AC adapter or battery pack is fed to the DC-DC converter and the system control servo (IC504), pin (53), via the IC link 1.0A (F501).

BATTERY on pin (53) is an analog input terminal used to monitor the input voltage from the battery. When the terminal voltage of the battery is 5.6V or more, the mark on the display window goes out; when 5.5V to 5.4V, the mark flickers; when 5.3V or less, the tape is forcibly stopped and then unloaded.

AC/DC on pin (23) is a power supply detection input which is High when the power is supplied from the battery pack or Low when the power is supplied via the AC adapter. (For details, refer to Section 5.1 AC/DC Detection Circuit.)

The following describes circuit operation when the power switch (S601) is turned on by using the timing chart in Figure 5-1. When the power switch (S601) is turned on, POWER on pin (50) goes Low and POW CON on pin (26) is driven High 160 ms later. This initiates operation of the DC-DC converter, with ±7V supplied to analog circuits and +5V supplied to the signal processor (IC515), LCD driver, and key input decoder (IC601). Figure 5-3 shows the internal circuitry of the DC-DC converter (CP501). When it starts operation, the oscillator circuit (IC1) begins to oscillate at a frequency of approximately 300 kHz, and transistors Q2 and Q4 are switched to output ±7V and +5V.

In the meantime, PWR CN1 on pin (25) goes High 560 ms after power-on and the digital filter (IC302), LCD driver, key input decoder (IC601), and other circuits are thereby cleared of reset, thus letting the entire system start operation.

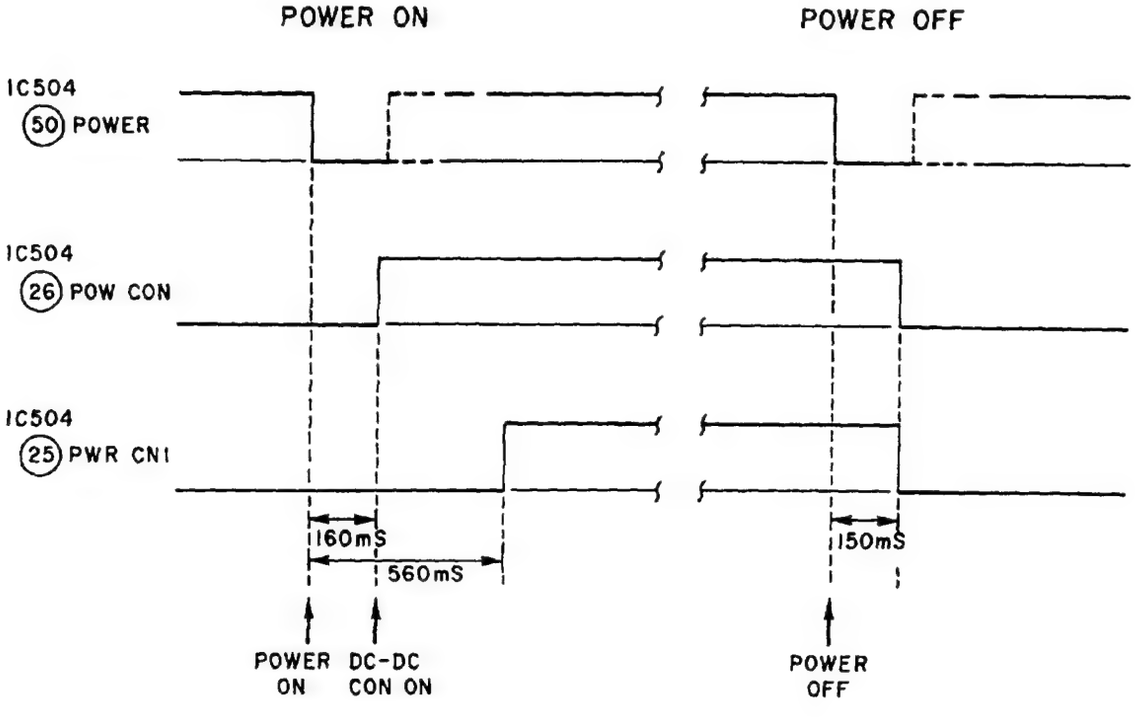


Figure 5-1. Power Supply ON/OFF Timings

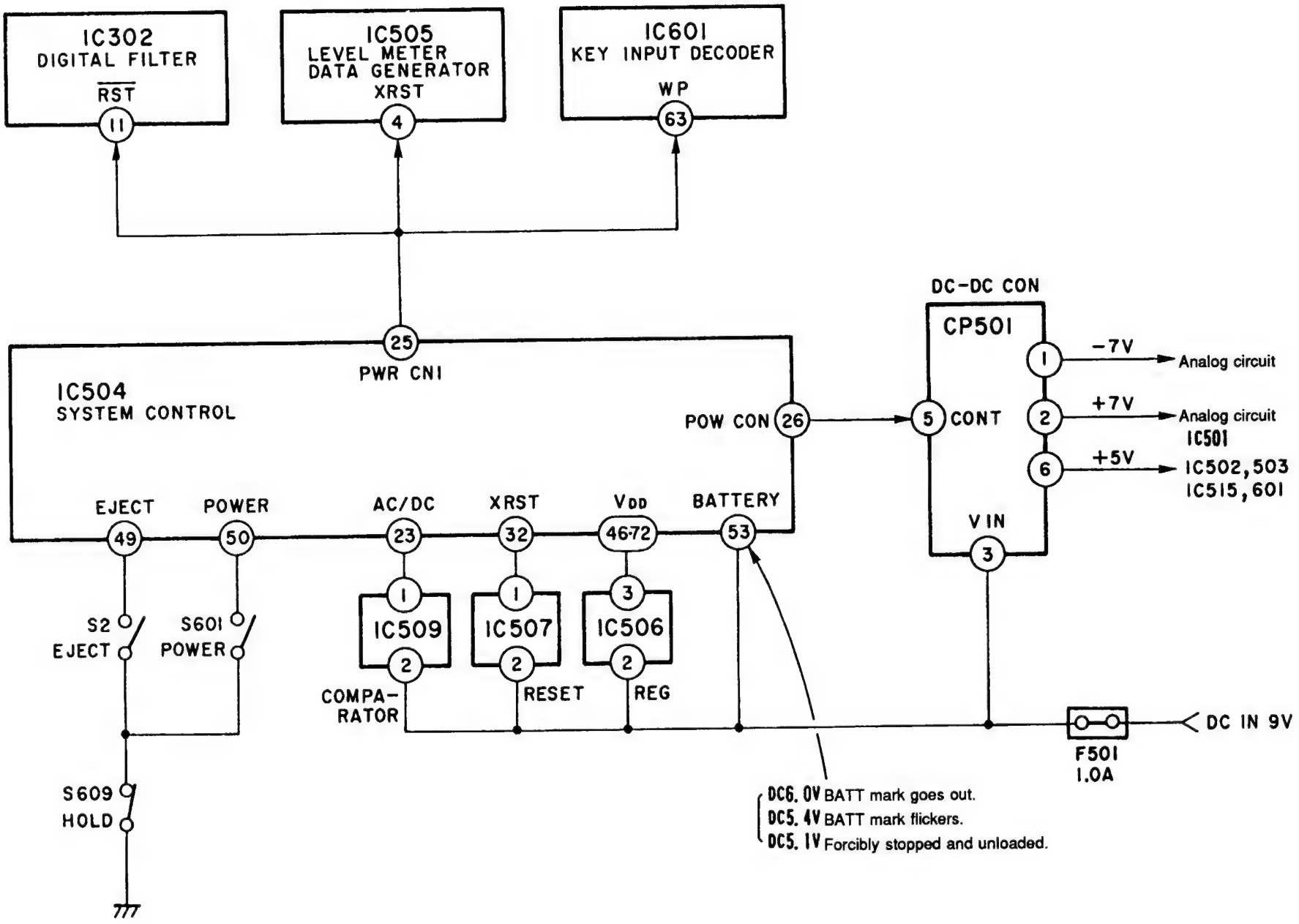


Figure 5-2. Block Diagram of Power Supply Circuit

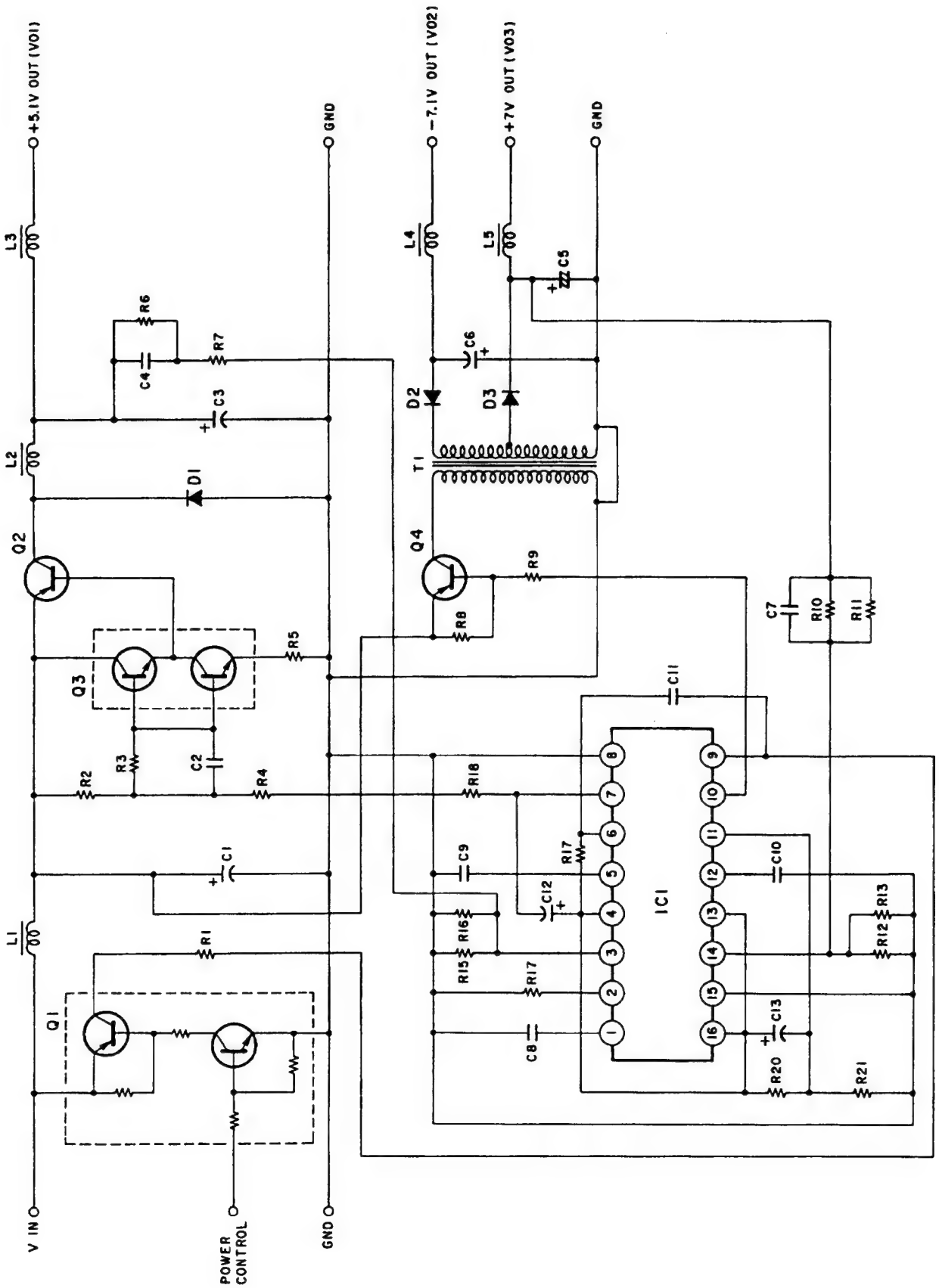


Figure 5-3. Internal Circuit of DC-DC Converter (CP501)

5.1 AC/DC Detection Circuit

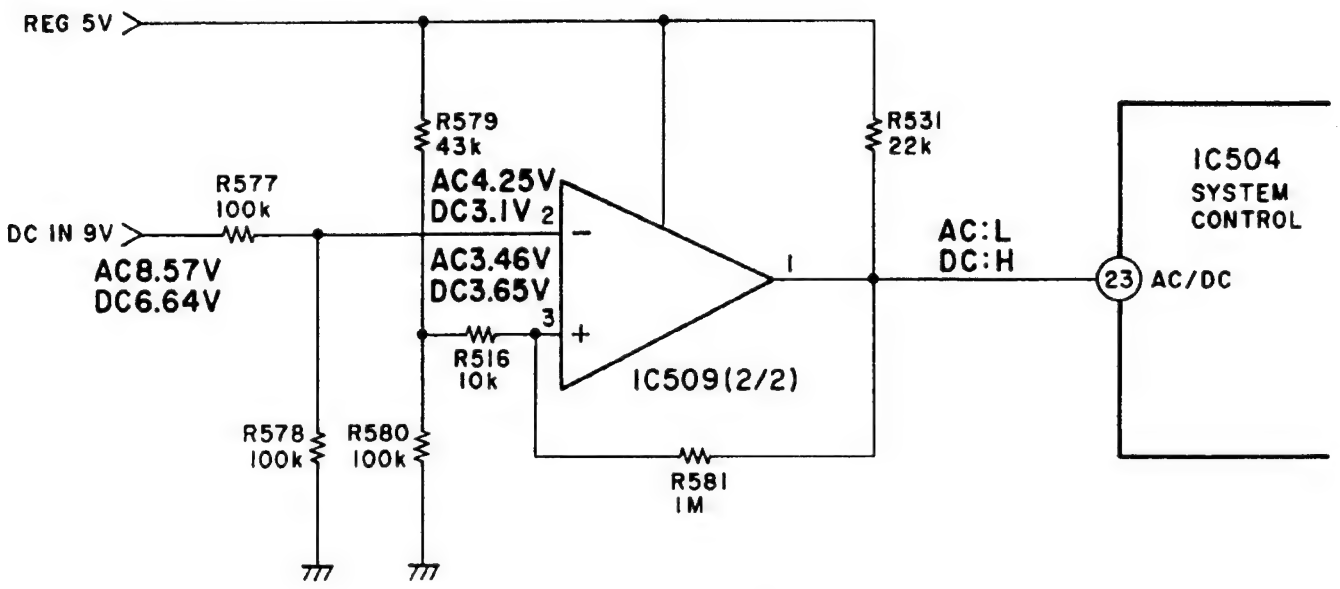


Figure 5-4. AC/DC Detection Circuit

The TCD-D3 has an auto power-off function which when operating with the battery pack, automatically turns off the power supply if continuously interrupted for 10 minutes or more. Therefore, it is necessary to know whether the power is supplied via the AC adapter or from the battery pack. The AC/DC detection circuit is used for this purpose.

The IC509 (2/2) configures a comparator where the reference voltage obtained by dividing REG 5V by resistor is connected to pin (3) and the voltage obtained by dividing DC IN by resistor is connected to pin (2).

When operating with the battery pack, the voltage applied to the system is lower by about 1.1V than when using the AC adapter. This voltage difference is used for AC/DC detection by the comparator.

Consequently, High is applied to the system control servo (IC504) pin (23) when operating with the battery pack; Low is applied when using the AC adapter.

6. Signal Circuit

6.1 Signal Processor (CXD2601AQ)

The CXD2601AQ integrates conventionally used three signal processor LSIs CXD1008 (ECC), CXD1009 (8-10 modulator/demodulator), and CXD1146 (digital I/O) into a single chip. Yet, it has almost all of the digital signal processing functions required for R-DAT systems.

Features

- Capable of recording in the following R-DAT modes:
  48 kHz 16 bits 2CH
  44.1 kHz 16 bits 2CH
  32 kHz 16 bits 2CH
  32 kHz 12 bits 2CH

- Has powerful error correction capability based on a new strategy.
  C1 first error detection
  C2 first error correction of up to five
  C1 second error correction of up to three
  C2 second error correction of up to six

- Contains a reproduction signal digital PLL circuit, eliminating the need for external components and adjustment.
- Incorporates a digital I/O circuit for use with serial copy management systems.
- Capable of after-recording of subcode data.
- Capable of high-speed search of subcode data.
- Automatically switches the mode (Fs, etc.) and applies mute during reproduction to reduce burdens on the microcomputer.
- Capable of variable speed reproduction.

Functions

- Recording signal modulation
- Reproduction signal demodulation (using digital PLL)
- Error correction code processing (parity generation, error detection and correction)
- Microcomputer interface (subcode processing, system control)
- A/D and D/A interface (including interpolation, mute processing, etc.)
- Digital interface
- RAM control
- Fs clock generation

Block configuration

The internal circuit of the CXD2601AQ is comprised primarily of the following eight blocks:

(1) D-PLL block
Digital PLL circuit for reproduction digital signal

(2) PB block
Reproduction data (10-8) demodulation and writing data to RAM
(3) REC block
Recording data (8-10) modulation, ATF generation, and recording data composition
(4) ECC block
C1/C2 parity generation based on R-DAT error correction format and C1/C2 error detection and correction
(5) SUB block
I/O of SUB code and other data to and from external microcomputer and control of D-I/O block
(6) ADA block
Generation of PCM data interleave address and internal data processing reference timing
(7) D-I/O block
AES-EBU D-I/O formatter circuit and Fs clock generation
(8) RMIF block
Address translation and access timing generation for access to external RAM

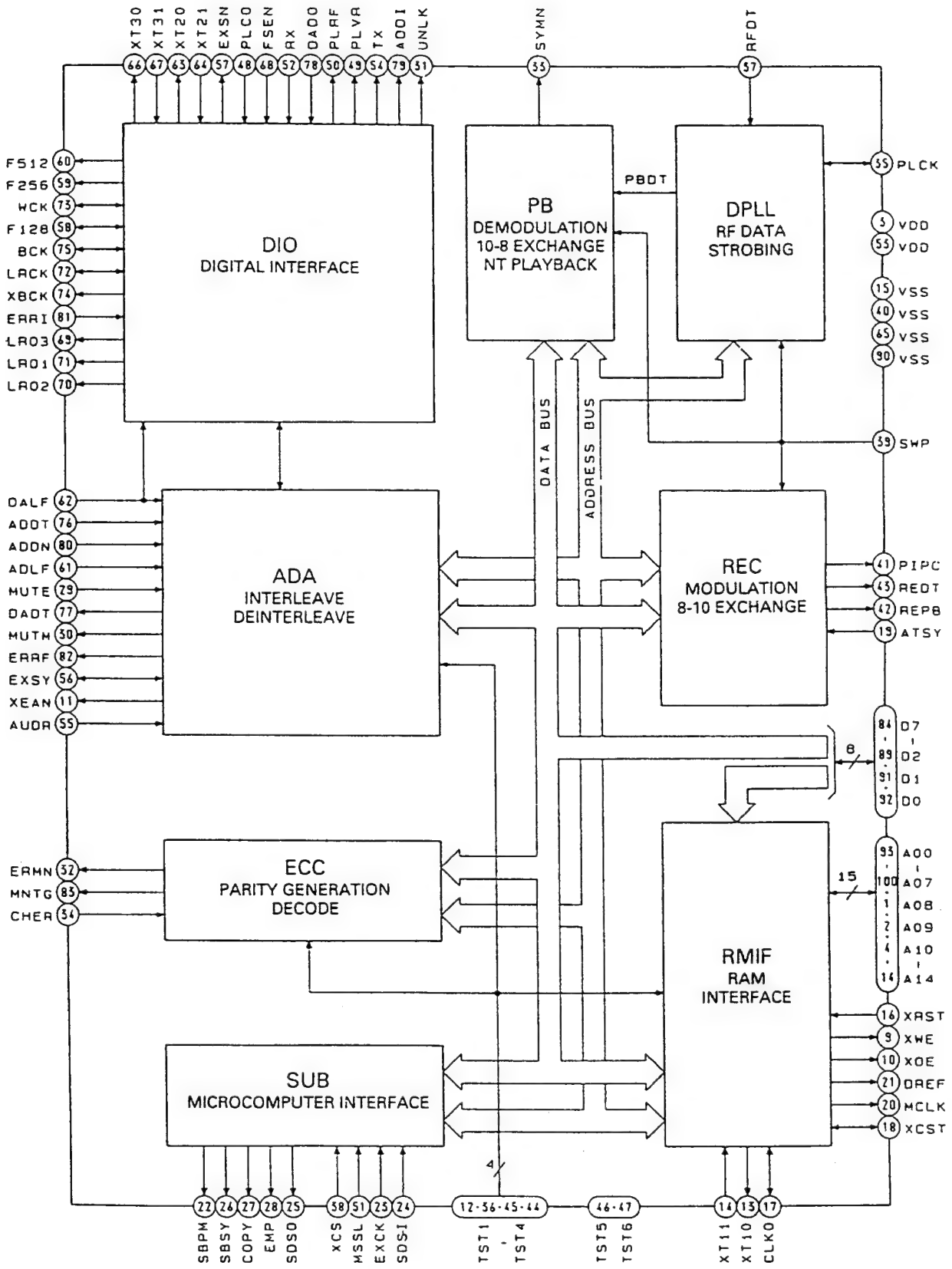


Figure 6-1. Internal Block Diagram of CXD2601AQ

6.2 Signal Flow during Recording

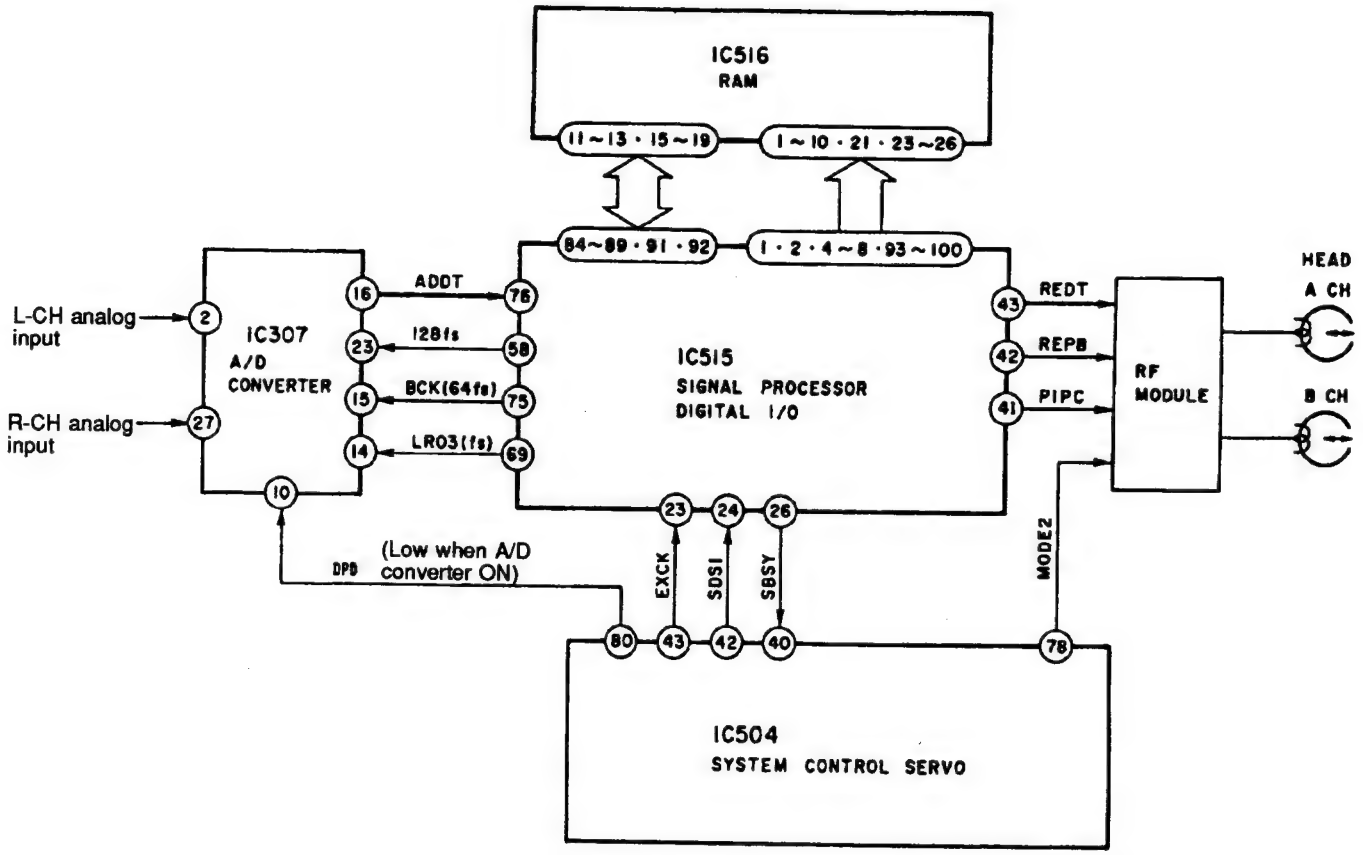


Figure 6-2. Flow of Recording Signal

The left- and right-channel analog signals input to the A/D converter (IC307) pins (2) and (27) are converted into 16- bit digital signals in the A/D converter and output alternately left and right channels from pin (16) for input to the signal processor (IC515) pin (76). On the other hand, subcode data such as absolute time and ID is serially input to the signal processor (IC515) pin (24). Each signal is interleaved and then appended with C1 and C2 parities in the signal processor (IC515) and RAM (IC516), respectively. The resulting signal is 8-10 modulated and appended with an ATF signal before being output from pin (43) to the RF module.

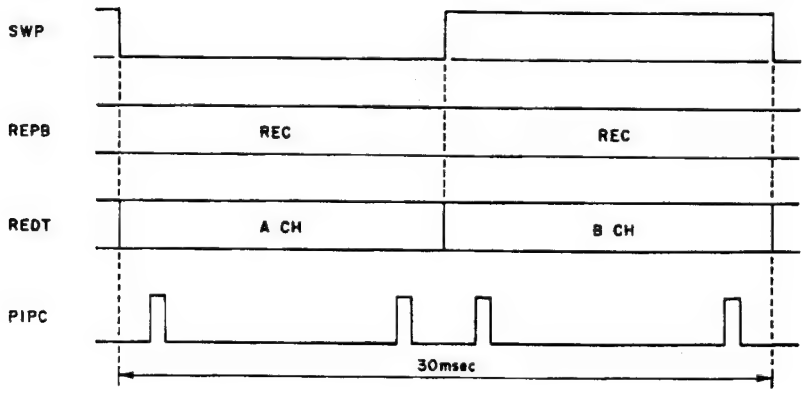


Figure 6-3. Signal Timing during Recording (SP Mode)

In the RF module, the recording data (REDT) is amplified by a recording amp and alternately sent to the heads A and B as recording signal synchronously with the switching pulse (SWP) as shown in Figure 6-3. The head REC/PB amp in the RF module is switched between recording and reproduction by MODE2 from the system control servo (IC504) pin (78) and record/playback discriminating signal (REPB) from the signal processor (IC515) pin (42). When both inputs are High, recording is assumed; when Low, playback is assumed. Also note that PIPC from the signal processor pin (41) indicates the ATF pilot signal recording area, and the ATF pilot signal recording level is set by this signal.

6.3 Signal Flow during Playback

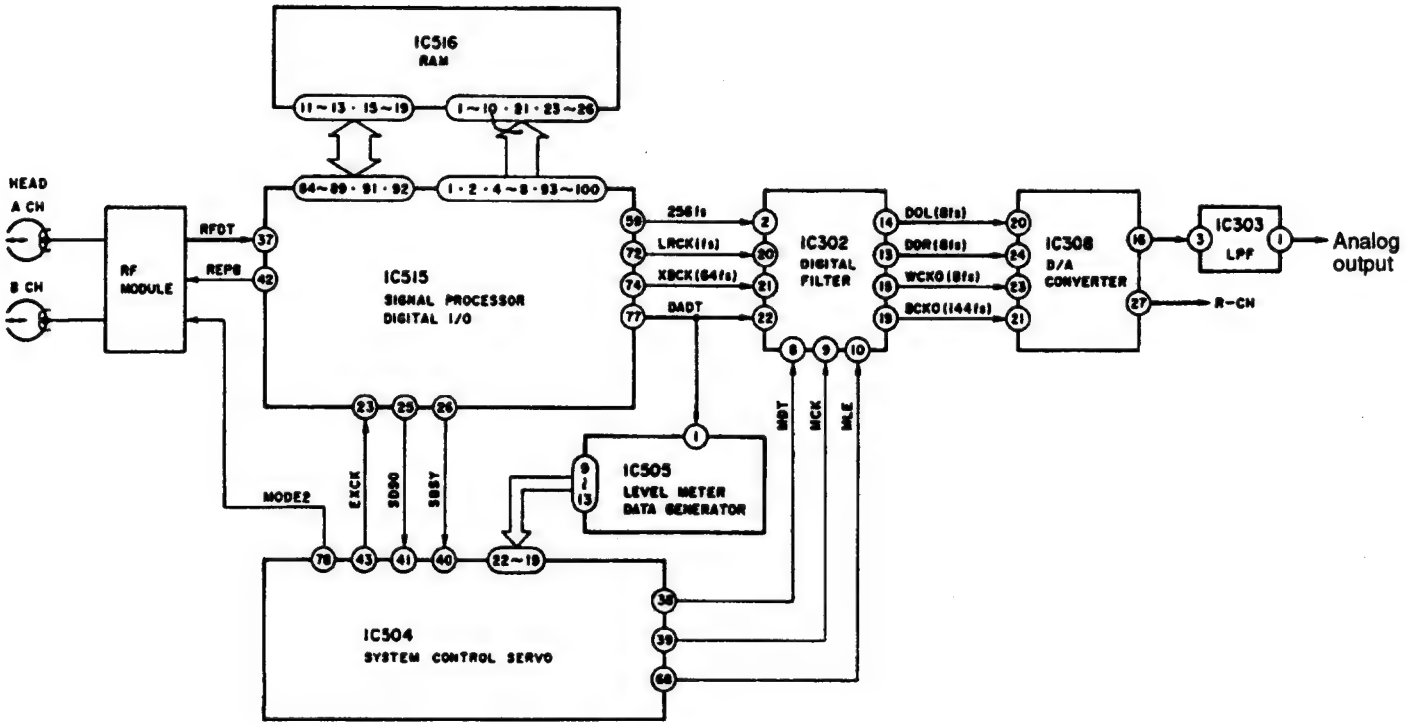


Figure 6-4. Flow of Reproduction Signal

The RF signals from the heads A and B are input to the RF module at the timing pulsed by SWP as shown in Figure 6-5 and amplified by the internal reproduction EQ amp.

Then, the RF signal is input to the signal processor (IC515) via pin (37) synchronously with the clock generated from RF data (RFDT) by the internal PLL circuit, and is 10-8 demodulated to reverse the recording process. The demodulated signal is deinterleaved by the signal processor and RAM (IC516) and subjected to error detection and error correction before being output to the next stage. The PCM data is output from pin (77) to the digital filter, and the subcode data is fed from pin (25) to the system control servo (IC504). In the digital filter, the 16-bit PCM data is 8-fold oversampled, converted into 18 bits, and subjected to digital filter computation before being output to the D/A converter, the left channel from pin (14) and the right channel from pin (13) respectively. In addition to these, the digital filter also has digital deemphasis and digital attenuator functions whose settings are made by signals input to the filter: mode set data (MDT on pin (8)), mode set clock (MCK on pin (9)), and mode set latch enable (MLE on pin (10)).

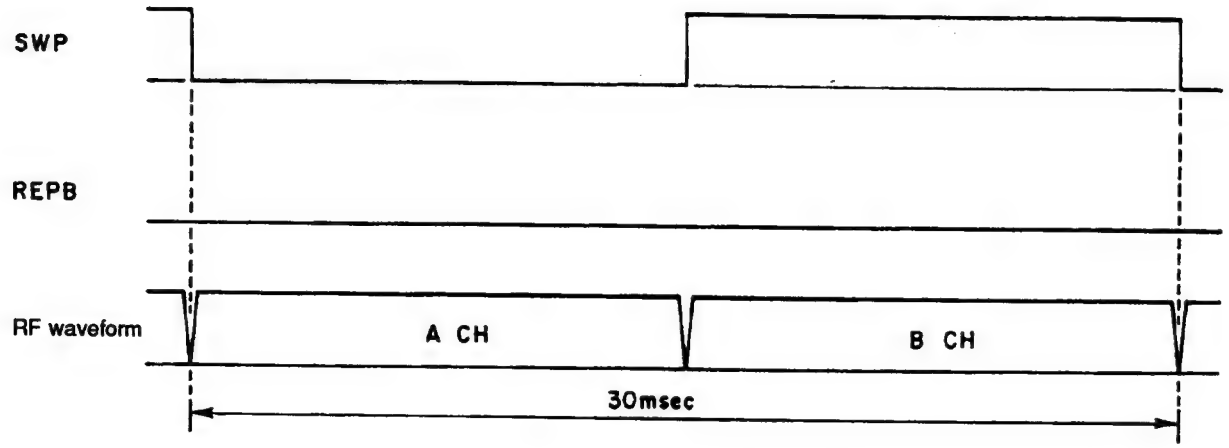
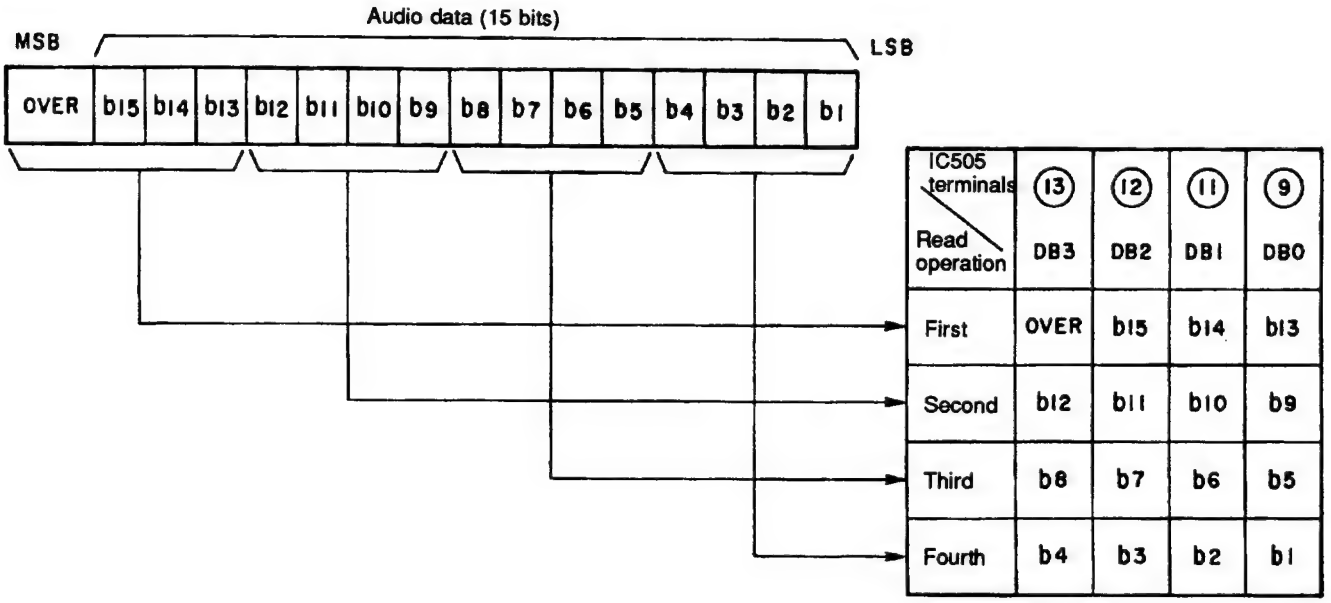


Figure 6-5. Signal Timing during Playback (SP Mode)

The level meter/data generator (IC505) sets the serial data from the signal processor pin (77) into the internal register in 16 bits as shown in Figure 6-6. This data is then output from the DB0-DB3 terminals to the system control servo (IC504) by the RD command from the system control servo pin (8) in four separate operations 4-bit parallel data at a time.



IC505 terminals / Read operation	(13) DB3	(12) DB2	(11) DB1	(9) DB0
First	OVER	b15	b14	b13
Second	b12	b11	b10	b9
Third	b8	b7	b6	b5
Fourth	b4	b3	b2	b1

Figure 6-6. Data Sent from Level Meter/Data Generator (IC505)

6.4 Internal Circuit of RF Module

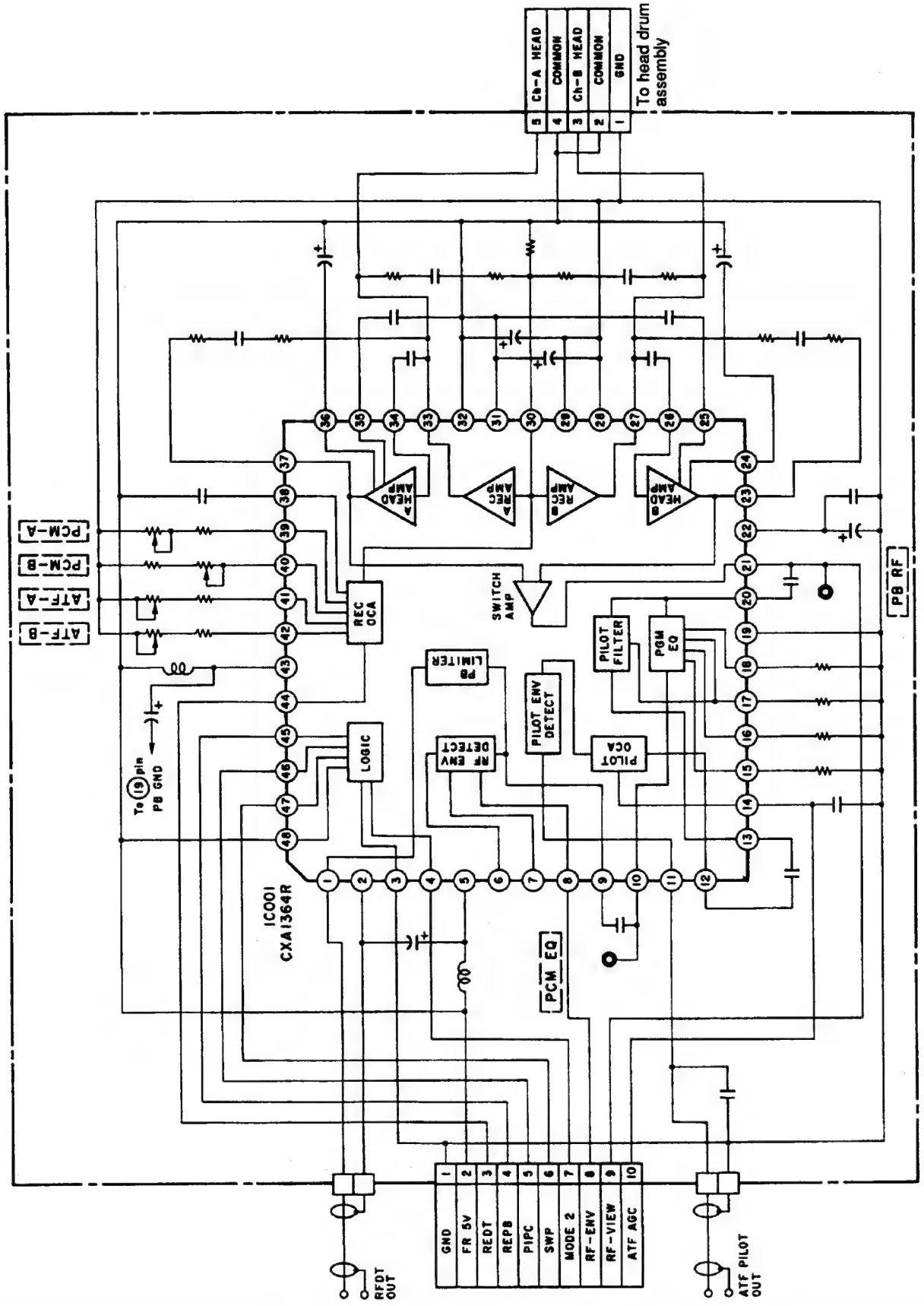


Figure 6-7. Internal Circuit of RF Module

7. System (Mechanical) Control

7.1 Outline

The TCD-D3 uses the CXP80524 chip as the main microcomputer. Broadly classified, its program consists of the following three blocks:

- Mechanical control (mecha deck control and internal mode generation)
- Serial data control (subcode data and display microprocessor I/O communications control)
- Servo control (drum and capstan software servo)

This microcomputer integrates all functions of the conventional main microcomputer, mecha microcomputer, reel microcomputer, and servo, as well as part of the ATF function into a single chip. Here, description is made mainly of mechanical control.

All mechanical controls are undertaken by the CXP80524 as shown in Figure 7-1. Mecha mode settings are done by the mode motor and rotary encoder, and loading/unloading are controlled by load/unload detection on the reverse side of the capstan motor and gear (loading). For FF, REW, and RVS, the mecha modes are maintained using a plunger by considering mecha deck characteristics.

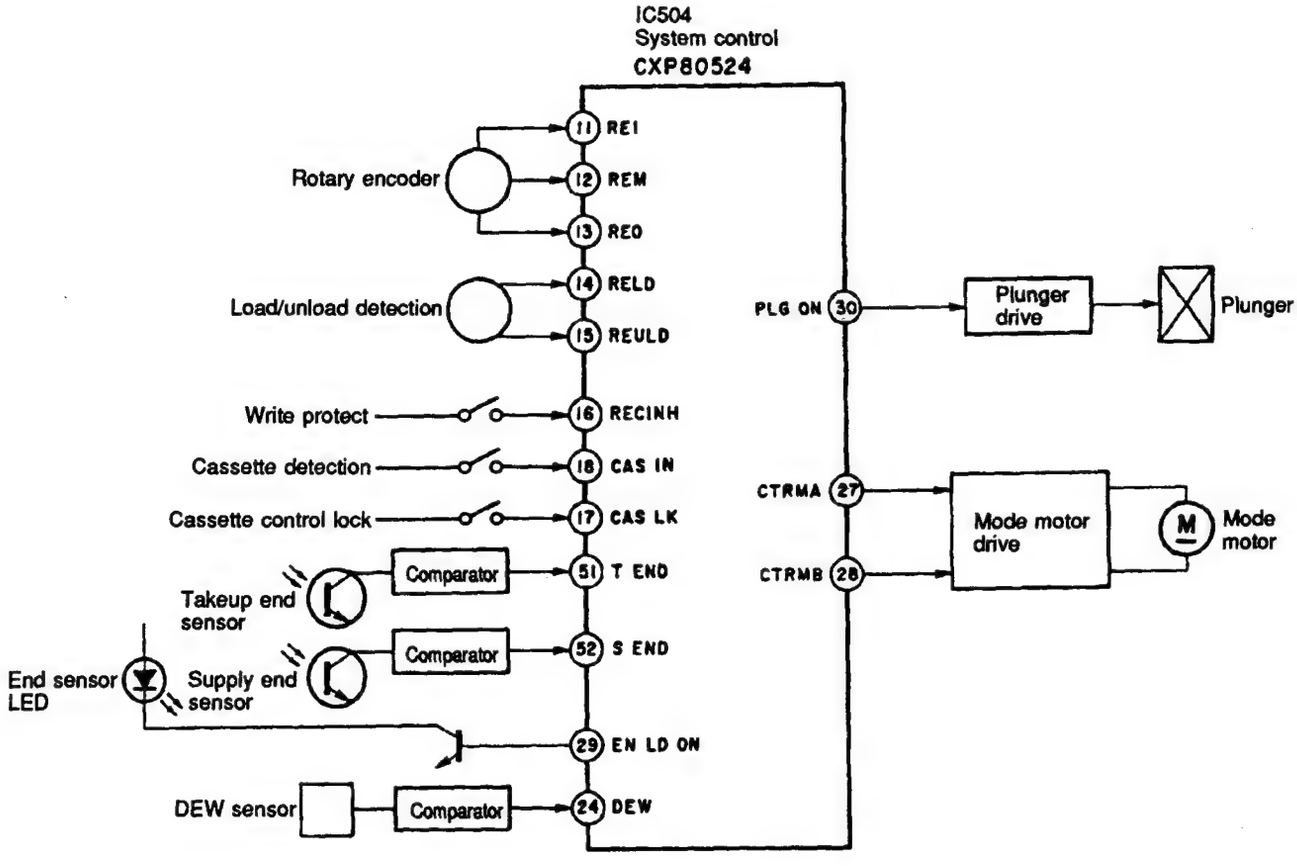


Figure 7-1. Schematic Diagram of Mechanical Control

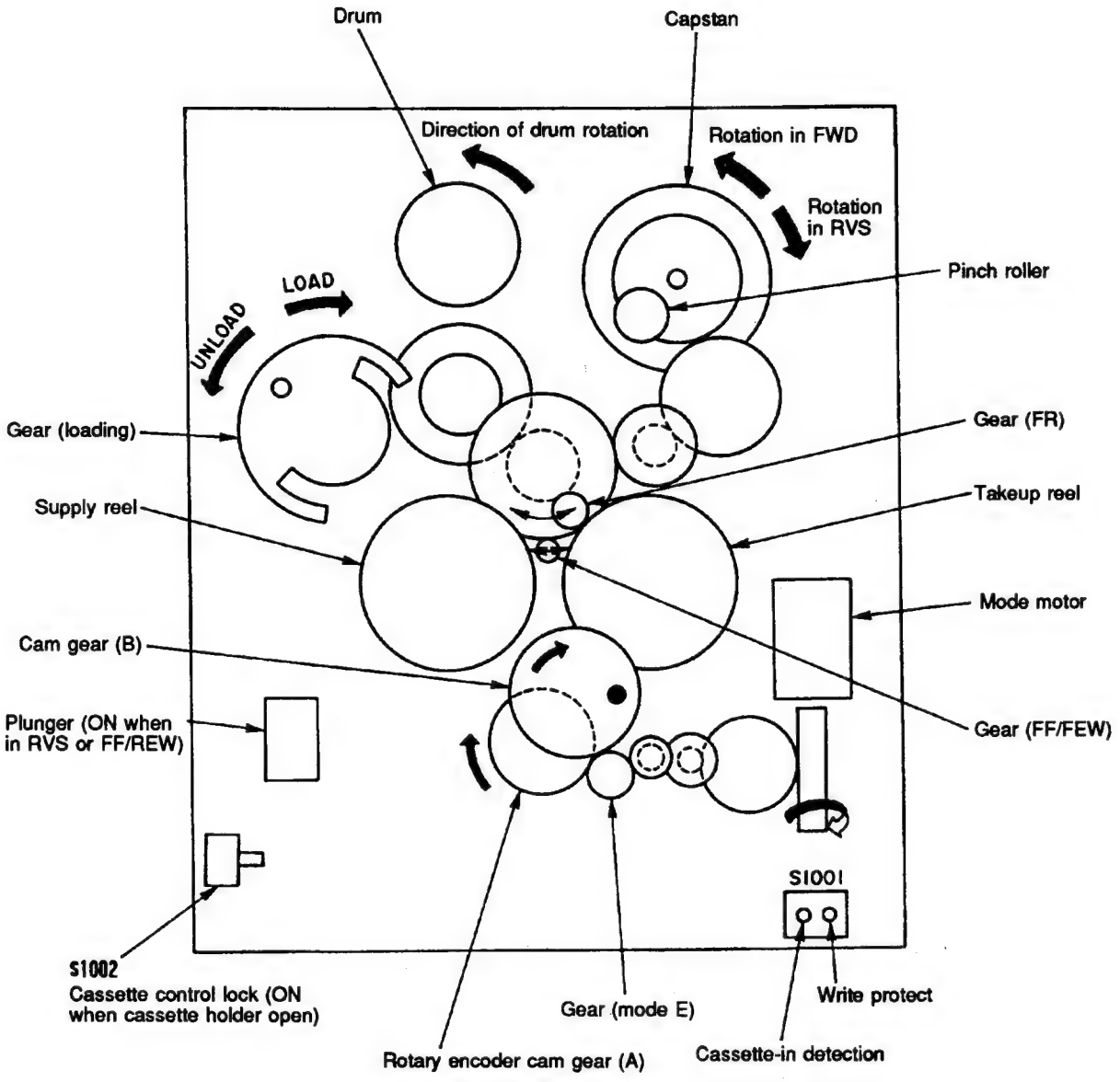


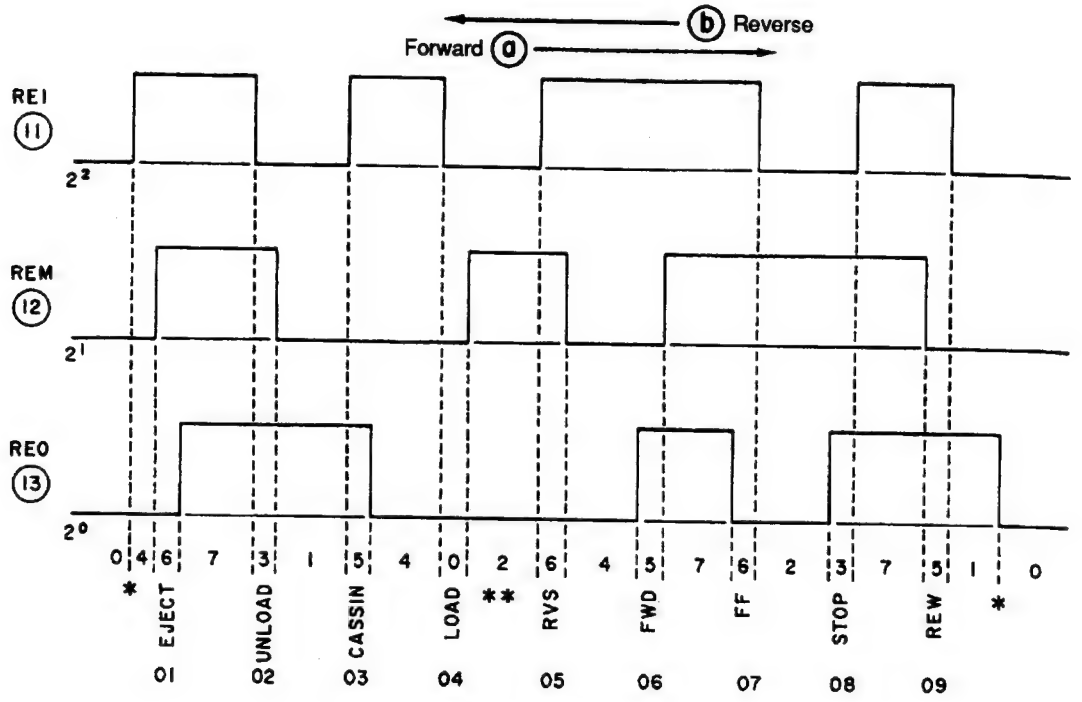
Figure 7-2. Locations of Main Mechanical Components on MD (Front)

Figure 7-2 shows the locations of the main mechanical components viewed from the front of the mecha deck. The mecha deck of the TCD-D3 uses three motors and three switches whose primary purposes are listed below.

- Drum motor: Drive the head drum.
- Capstan motor: Feed tape (in FWD and RVS), drive the takeup and supply reel bases, and load/unload tape.
- Mode motor: Set the mecha modes.
- S1001 (right): Detect the write protect hole. (ON when write protect hole closed)
- S1001 (left): Determine whether a cassette is inserted. (ON when cassette inserted)
- S1002: Detect the cassette control lock. (ON when cassette holder open)

In addition to the above, the mecha deck has an end sensor LED, end sensor phototransistor (one each on the takeup and supply sides), and a DEW sensor whose resistance increases as humidity increases.

7.2 Rotary Encoder Pattern and Control



* Transition beyond this point is mechanically inhibited.
** Mechanical transition beyond RVS is inhibited unless loading is completed.

Figure 7-3. Rotary Encoder Pattern

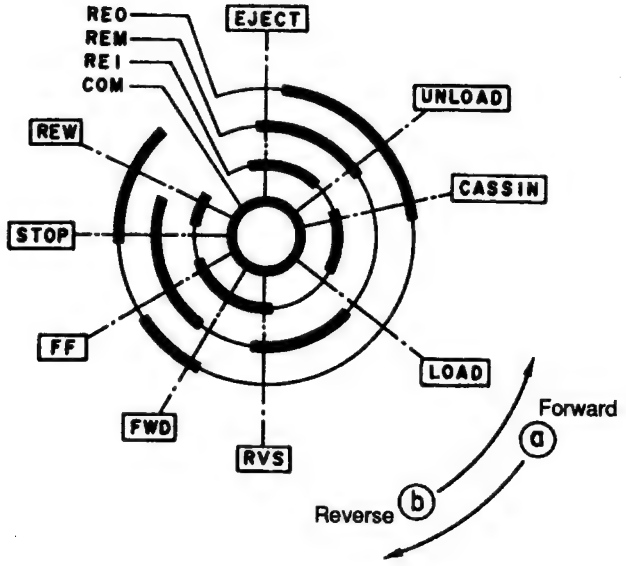


Figure 7-4. Electrode Pattern on the Reverse Side of Rotary Encoder

The rotary encoder (assigned a component name "cam gear A") is driven by the mode motor via four relay gears to set nine kinds of mecha modes from EJECT to REW as shown in Figure 7- 4. The encoder position is controlled by controlling the mode motor according to the targets set by mecha control. Four encoder control bits are used, the inner most bit of which is common (V_{CC} = 5V), and the encoder position is recognized and controlled using the three other bits. The actual method of control is such that each mode in Figure 7- 3 is assigned numbers 01, 02, ... 09 sequentially from left to right (beginning with EJECT). This number serves as a target for transition to the desired mode, and as a reference to determine the direction of rotation whether forward or reverse.

Let us assume transition from STOP to FWD, for example. Since the current position is 08 and the target is 06, the motor is turned in reverse and stopped when number 06 is reached. In actual operation, mode numbers are determined using the preceding and current codes as one set. To take EJECT as an example, 6 comes after 4 (64 as a set) when rotating in forward; 6 comes after 7 (67) when rotating in reverse so that when this pattern is encountered, EJECT, that is, number 01, is assumed. If overrun past the target, the motor is decelerated and the position is moved in the opposite direction by pulse drive.

7.3 Detecting Rotary Encoder Position

Encoder positions are normally detected by sampling the status of the control bits at a 1.74ms period and assuming that the position is reached when two sampled states match. When the desired position is detected, the mode motor is forcibly stopped and an overrun detection timer (150 ms) is activated. Detection of encoder positions is continued (to detect overrun) even while the timer is active and when the encoder is at the desired position after the timer times out (after an elapse of 150 ms), encoder transition is assumed to have been completed. However, if the encoder position is not the target position, an overrun is assumed and positions are set over again and the mode motor is restarted. In this case, the mode motor is driven in the direction opposite the previous direction of rotation and a different method of drive is used. In place of the previous method of control where a constant voltage is applied, the motor is now driven by a pulse that periodically turns voltage on and off as shown in Figure 7-5.

After restart, position detection is limited to five times of check so that if the motor cannot stop at the target position after five times of check, encoder transition is terminated at the fifth detected position.

If the target position cannot be located by encoder position detection within five seconds after the mode motor is first started, an error is assumed and a transition to emergency operation takes place.

If an overrun is encountered during encoder position detection, the mode motor is turned in reverse at that point in time and position codes are set over again and position detection is restarted.

For FF, REW, RVS x 1, RVS x 3, RVS x 16, RVS x 25 (fast REV), and FWD x 25 (fast CUE), operation must be controlled by turning the plunger on and off. This plunger control is required when a position to turn it on or off is detected or an overrun is encountered.

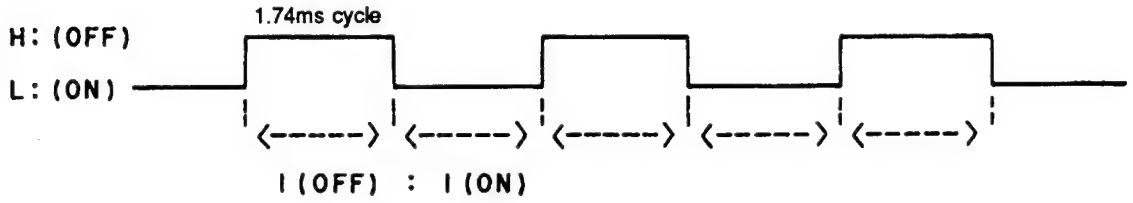


Figure 7-5. Mode Motor ON/OFF Pattern (Pulse Drive) in Encoder Overrun

7.4 Detecting Load/Unload Completion

Loading and unloading are done by turning the gear (loading) in Figure 7-2 in forward or reverse. This gear is driven by the capstan motor via four auxiliary gears so that a cassette is loaded into position as the capstan motor rotates in forward (FWD) and unloaded as the capstan motor rotates in reverse (RVS). Completion of loading or unloading is detected using two gear (loading) control bits (the outer circumference bit is common, V_{CC} = 5V). Loading is assumed to have been completed when the RELD bit is High, and unloading is assumed to have been completed when the REULD bit is High as shown in Figure 7-6. If transition is not completed within four seconds after the capstan motor is started, an error is assumed and a transition to emergency operation takes place. Figure 7-7 shows the timing of each signal on the system control servo (IC504) for a series of operation from TAPE IN to EJECT KEY ON.

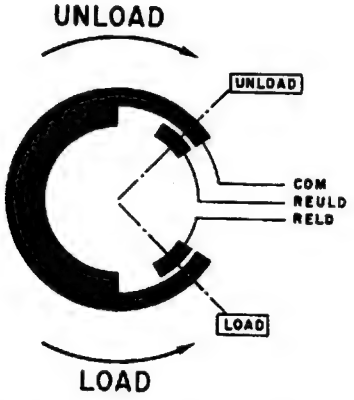


Figure 7-6. Electrode Pattern on Reverse Side of Gear (Loading) (as viewed from the reverse side of MD)

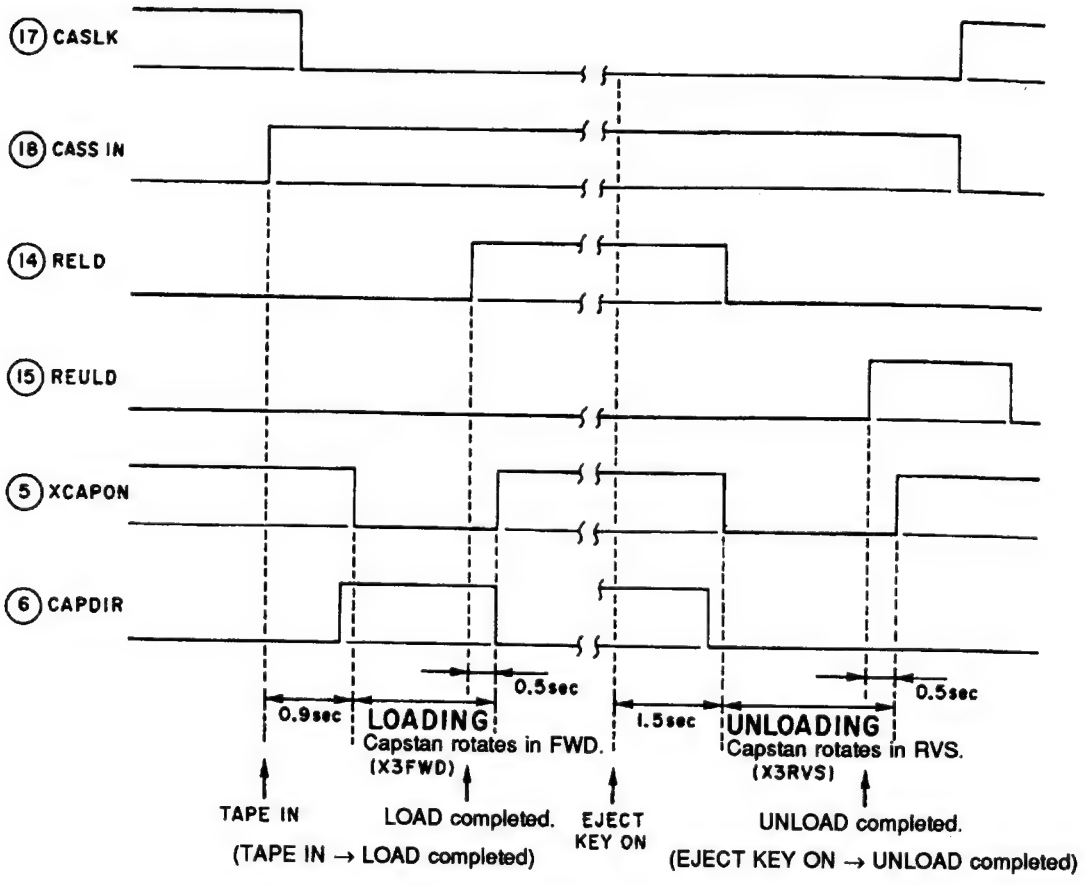
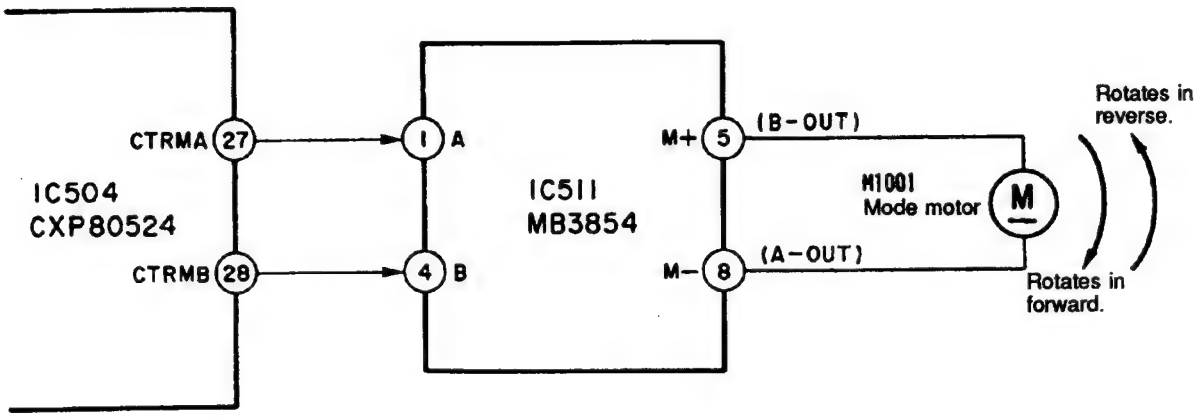


Figure 7-7. Load/Unload Timings

7.5 Mode Motor Control

The mode motor drive (IC511 MB3854) selects each mode (A, B, C, or D) by controlling two bits, A-IN and B-IN. The mode motor is started in mode B or C and forced to stop by applying brakes in mode A. When the mode motor is not in operation, mode D is selected with the terminal left open to reduce current consumption. Figure 7-9 shows the input/ output timing of the mode motor drive (IC511) when EJECT KEY is turned on while tape is not in place.



Mode Motor Control Matrix (MB3854)

Mode	A IN (1)	B IN (4)	M+ (5)	M– (8)	OUT PUT
A	1	1	L	L	Brakes applied
B	1	0	H	L	Turned in forward
C	0	1	L	H	Turned in reverse
D	0	0	-	-	Terminal open

Figure 7-8. Mode Motor Control Circuit

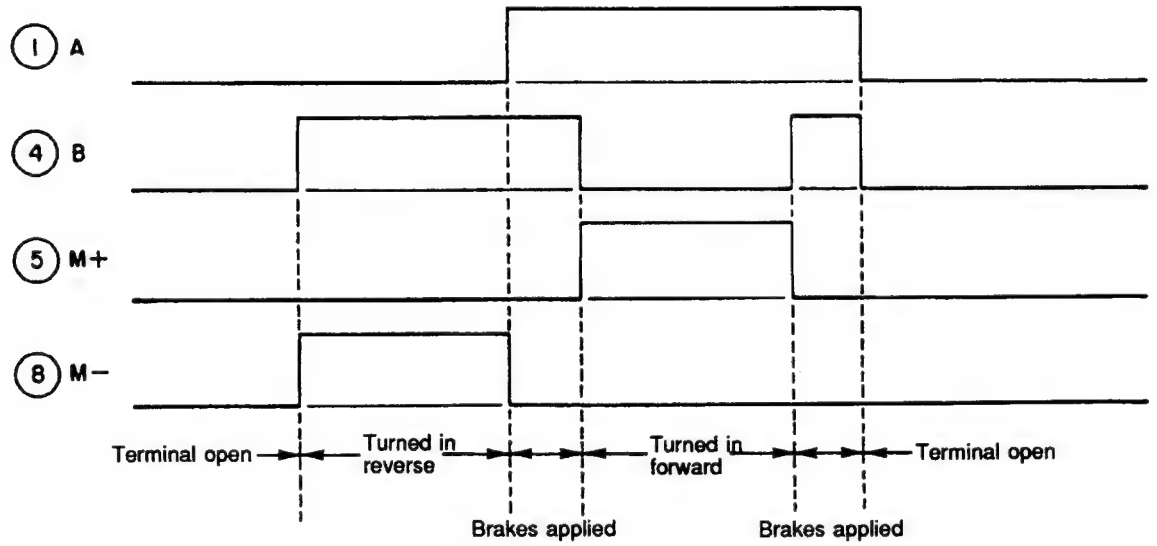
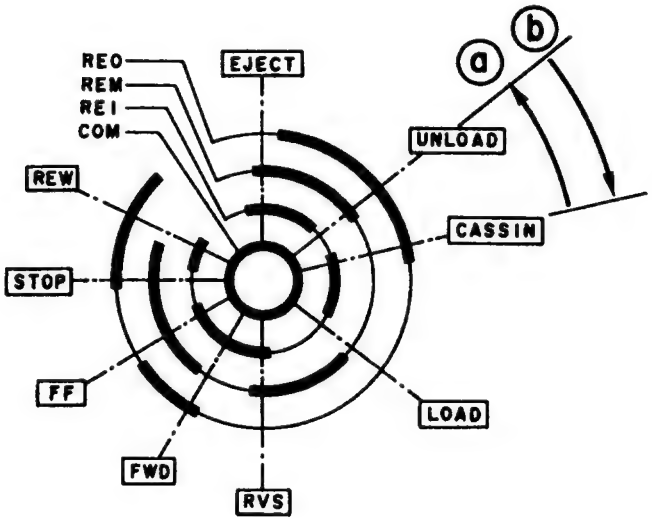


Figure 7-9. Mode Motor Drive Control (EJECT Without Tape)

7.6 Transition Timing in Each Mode

7.6.1 POWER ON

This is an operation performed only one time when the battery is fitted into place or the AC adapter is connected while tape is not in place.
(This operation is not executed for the second or subsequent power-on. The diagram below shows an example where the encoder before POWER ON is positioned at CASS IN.)



When powered on, the encoder position is set for the UNLOAD mode ((a)) to perform UNLOAD operation to reset the mecha deck. The encoder is then moved up to the CASS IN position to terminate transition ((b)). In this mode, therefore, the encoder performs the following operations: position before POWER ON → UNLOAD → CASS IN.

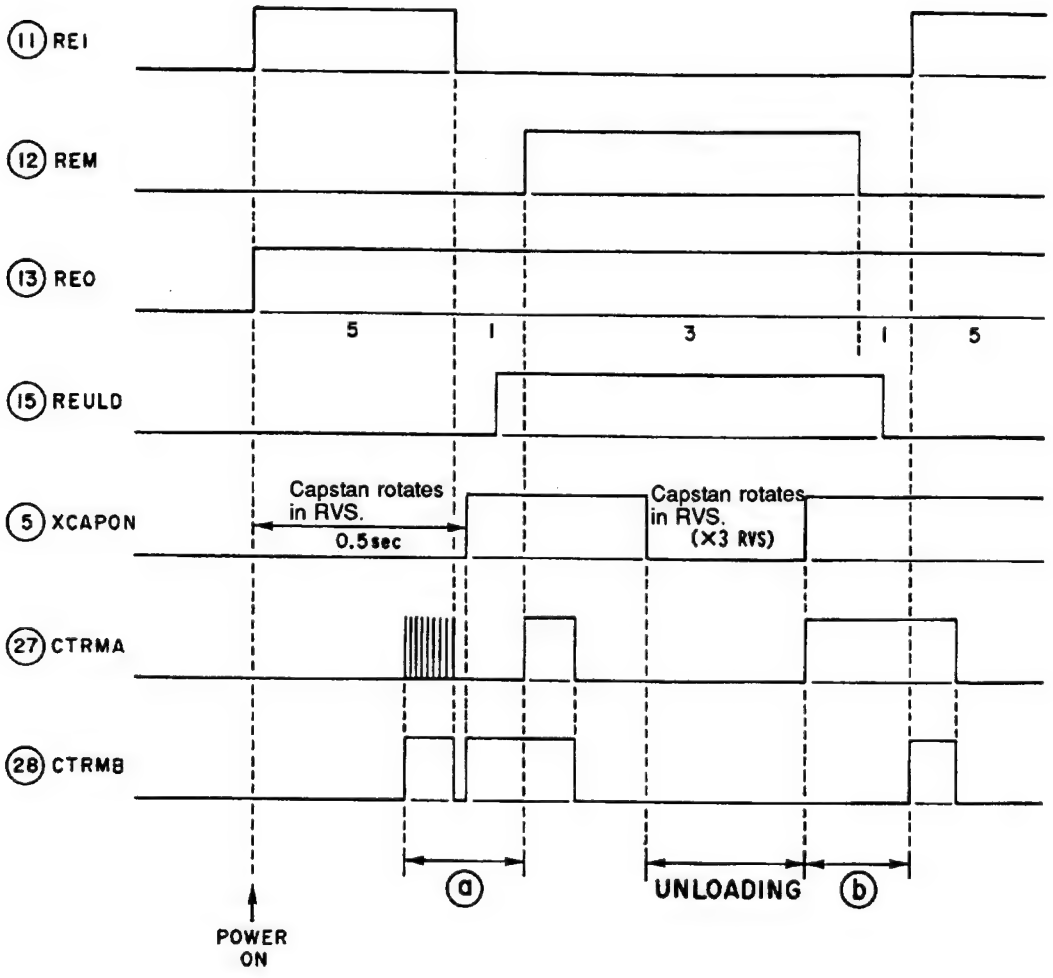
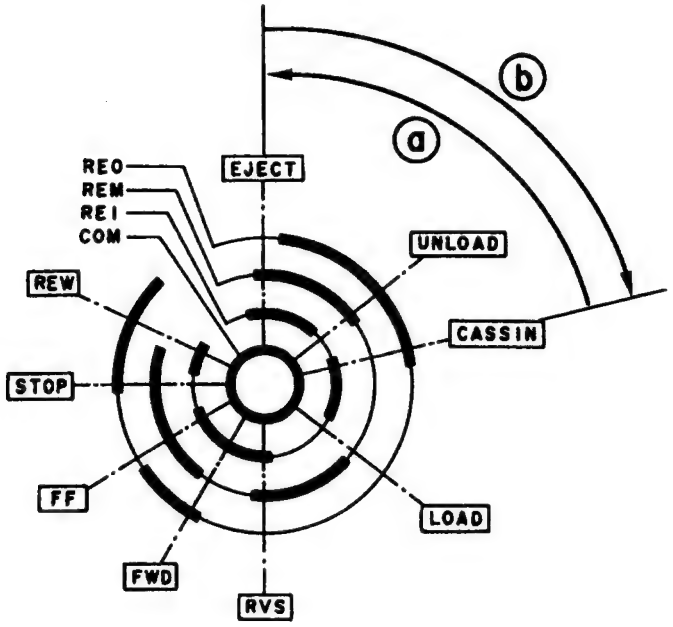


Figure 7-10. POWER ON

7.6.2 EJECT

- **A mode where no tape is in place after POWER ON**



In the EJECT mode, the encoder is first moved from the CASS IN to the EJECT positions ((a)). This causes the cam gear (B) to rotate and the cassette holder to open, and the cassette control lock switch (S1002) to be pressed. Then, the encoder is moved back to the CASS IN position to terminate transition ((b)). In this mode, therefore, the encoder performs the following operations: CASS IN → EJECT → CASS IN.

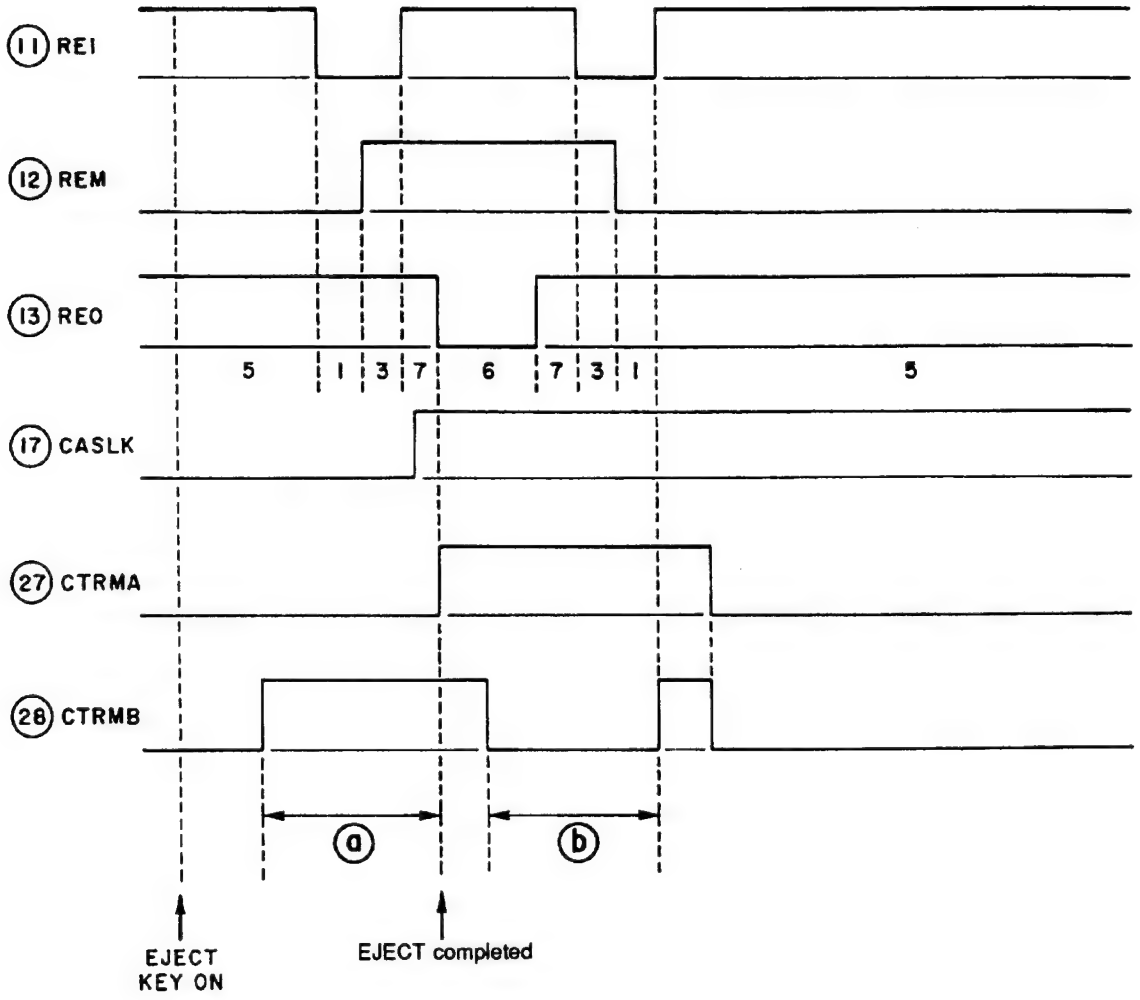


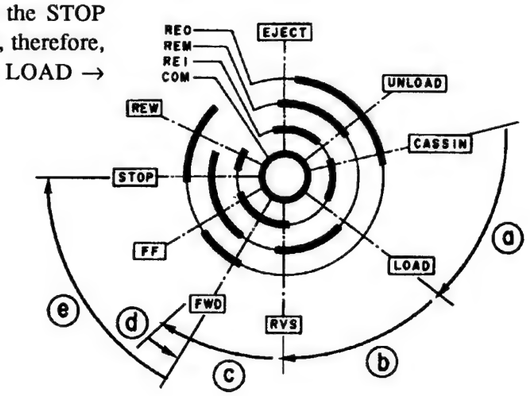
Figure 7-11. EJECT

7.6.3 CASS IN → STOP

- **A mode where tape is set into place when the cassette holder is open and then the holder is closed.**

Transition from the CASS IN to the STOP modes occurs in the following way. First, the cassette-in switch (S1001) turns on and the cassette control lock switch (S1002) turns off, causing the encoder to move to the LOAD position ((a)). After this transition is completed, the capstan motor is rotated in forward at 3 times normal speed to load the cassette into place. Next, the encoder is turned until the RVS position is reached ((b)) and tape is run in reverse at 16 times normal speed for about one second to read the main ID, subcode, and other data.

Then, the encoder is further moved to the FWD position ((c)) so that tape is wound back to the position where loading was completed at 16 times normal speed ((d)). After that, the encoder is moved up to the STOP position to terminate the encoder transition ((e)). In this mode, therefore, the encoder performs the following operations: CASS IN → LOAD → RVS → FWD → STOP.



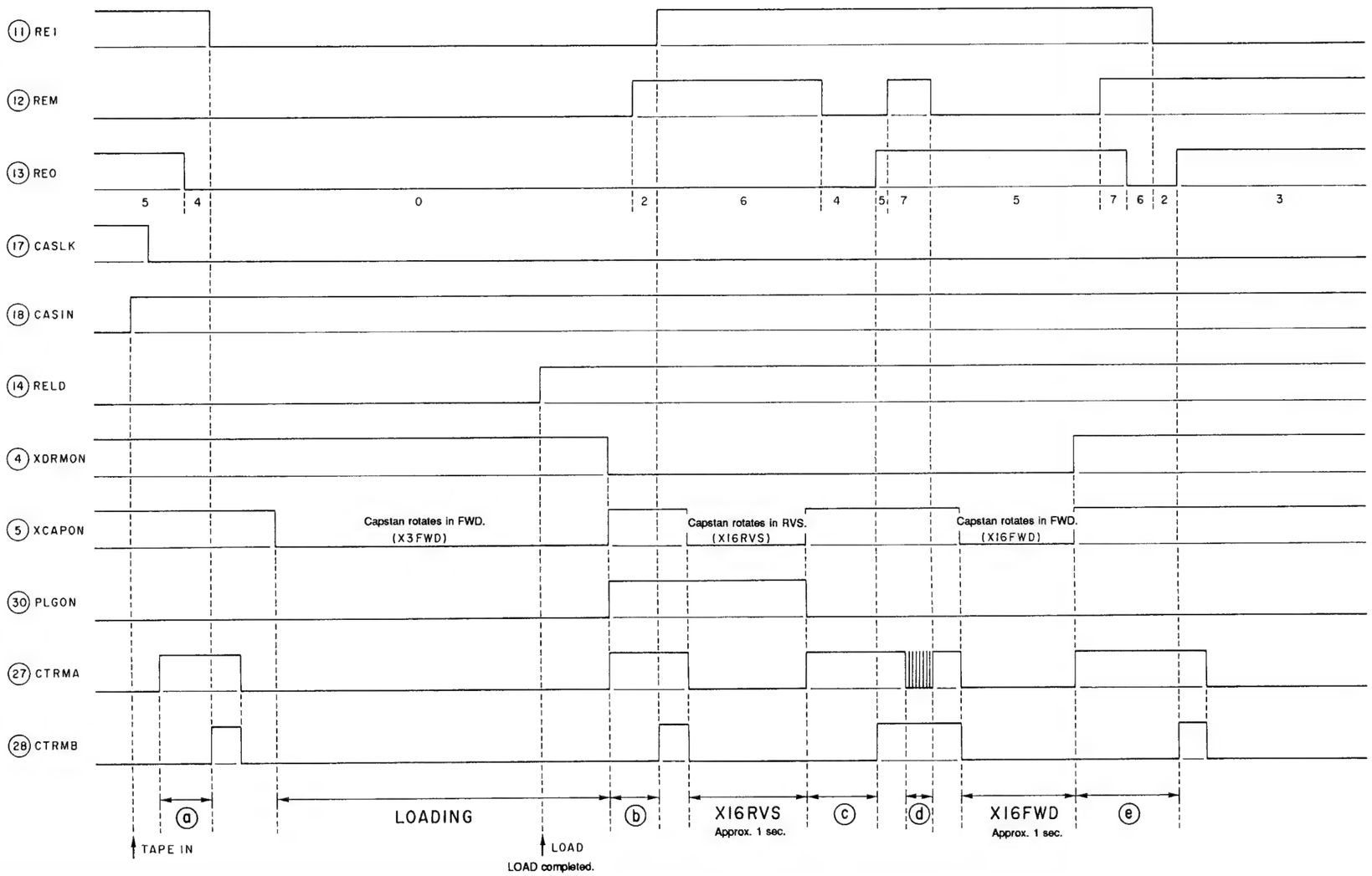
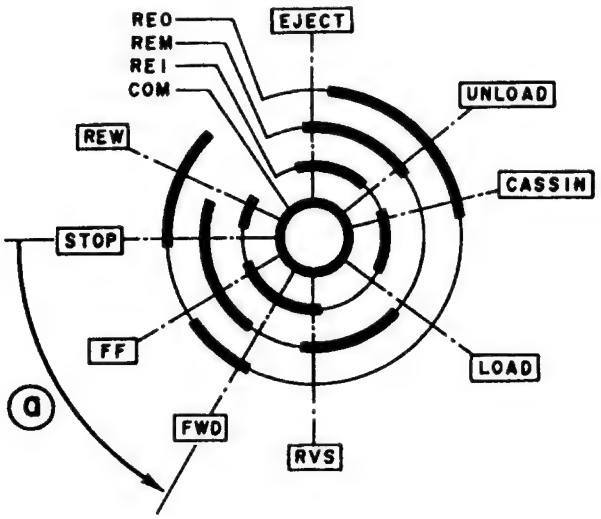


Figure 7-12. CASS IN → STOP

7.6.4 STOP → FWD



Transition to the FWD mode is terminated by detection of the encoder's FWD position ((a)). When this is done, the FWD- mode mecha settings are made by pressing the pinch roller against the capstan shaft and releasing the takeup and supply reel brakes. The capstan motor turn-on timing is such that the motor is started immediately after the encoder detected the FWD position.

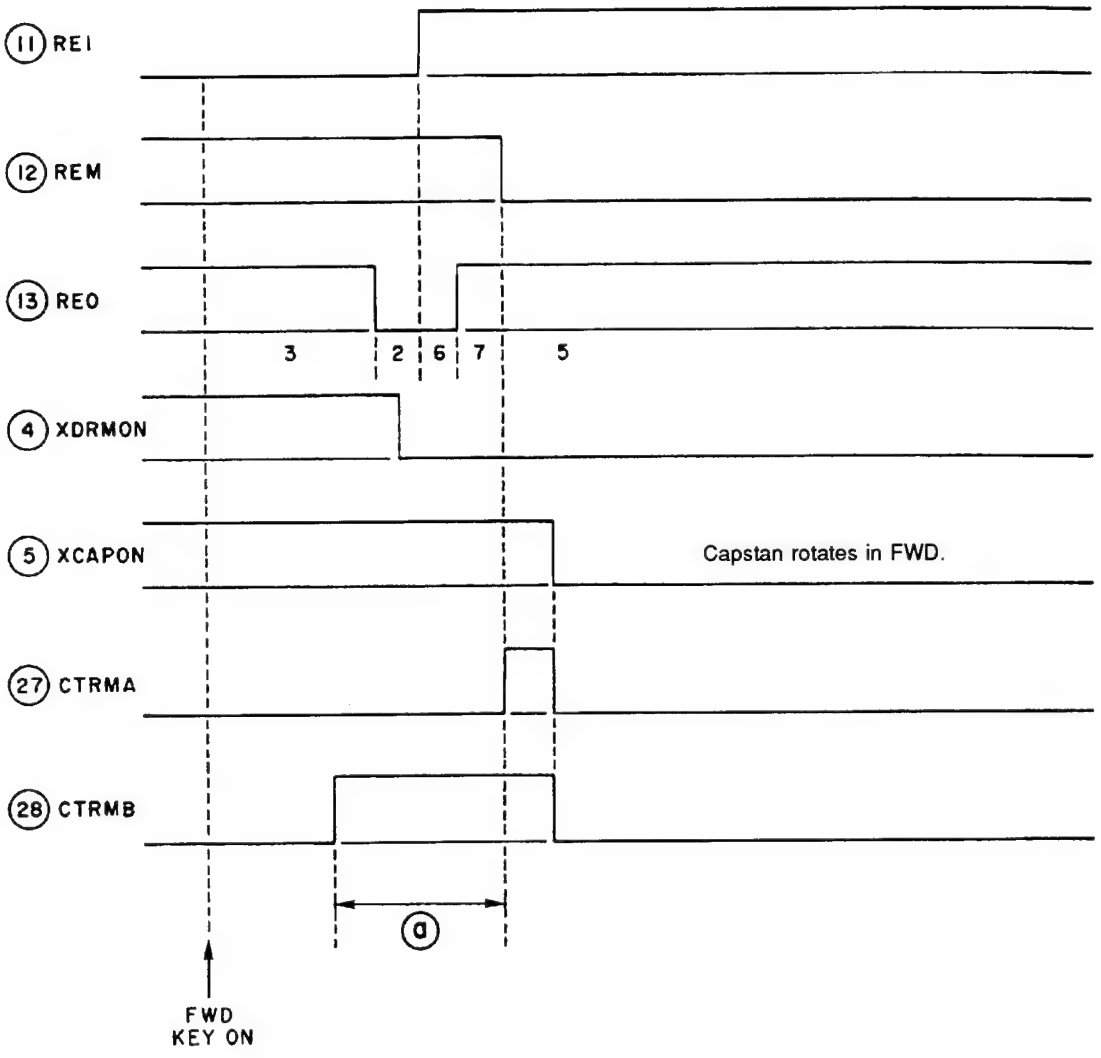
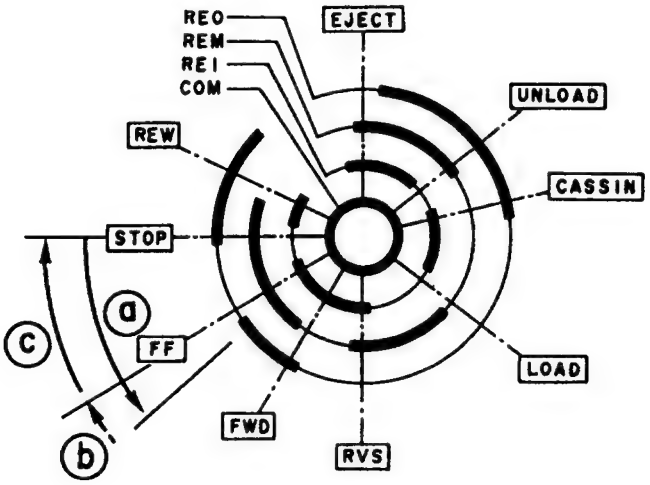


Figure 7-13. STOP → FWD

7.6.5 STOP → FF



Transition to the FF mode is accomplished by first moving the encoder to the FF position to pull the plunger and have the mecha deck mechanically locked to the FF mode ((a)). Then, the encoder is moved back to the STOP position to terminate its transition ((c)). The capstan motor turn-on timing is such that the motor is started after the encoder position is moved from FF back to STOP. In this mode, therefore, the encoder performs the following operations: STOP → FF → STOP.

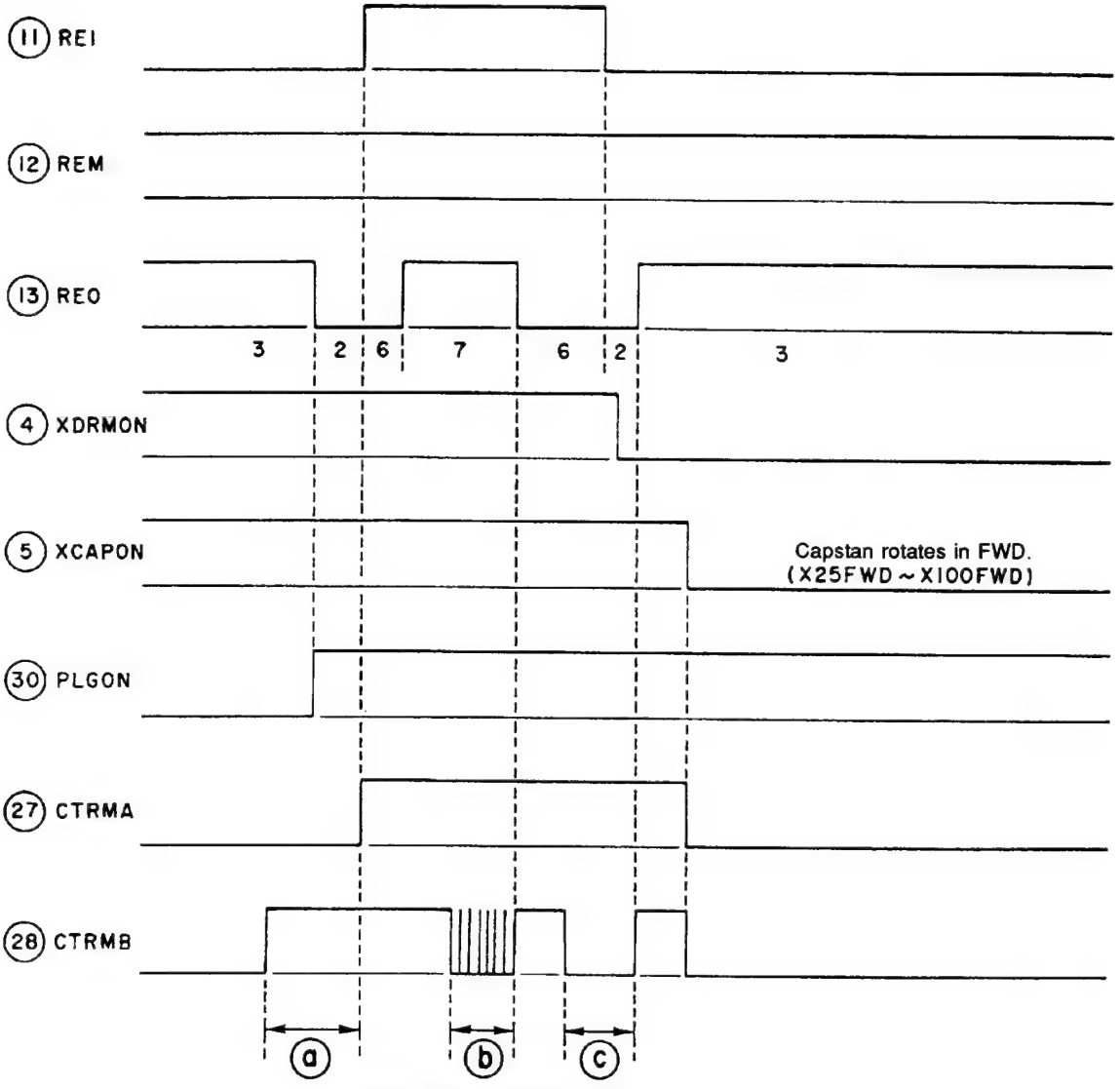
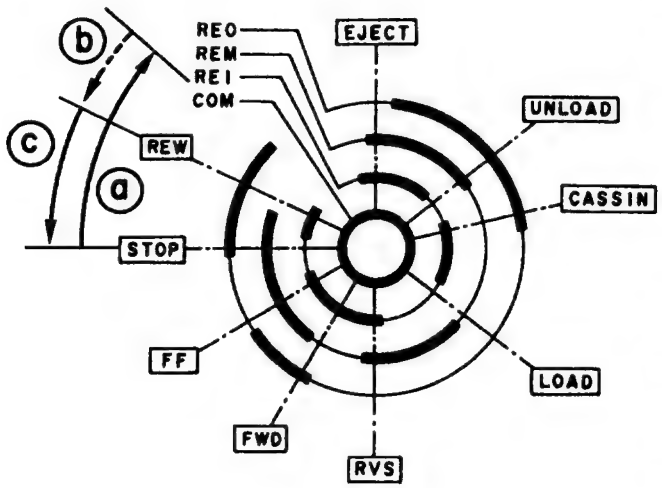


Figure 7-14. STOP → FF

7.6.6 STOP → REW



Transition to the REW mode is accomplished in the same way as for transition to the FF mode by first moving the encoder to the REW position to pull the plunger and have REW mechanically locked ((a)). Then, the encoder is moved back to the STOP position to terminate its transition ((c)). The capstan motor turn-on timing is such that the motor is started after the encoder position is moved from REW back to STOP. In this mode, therefore, the encoder performs the following operations: STOP → REW → STOP.

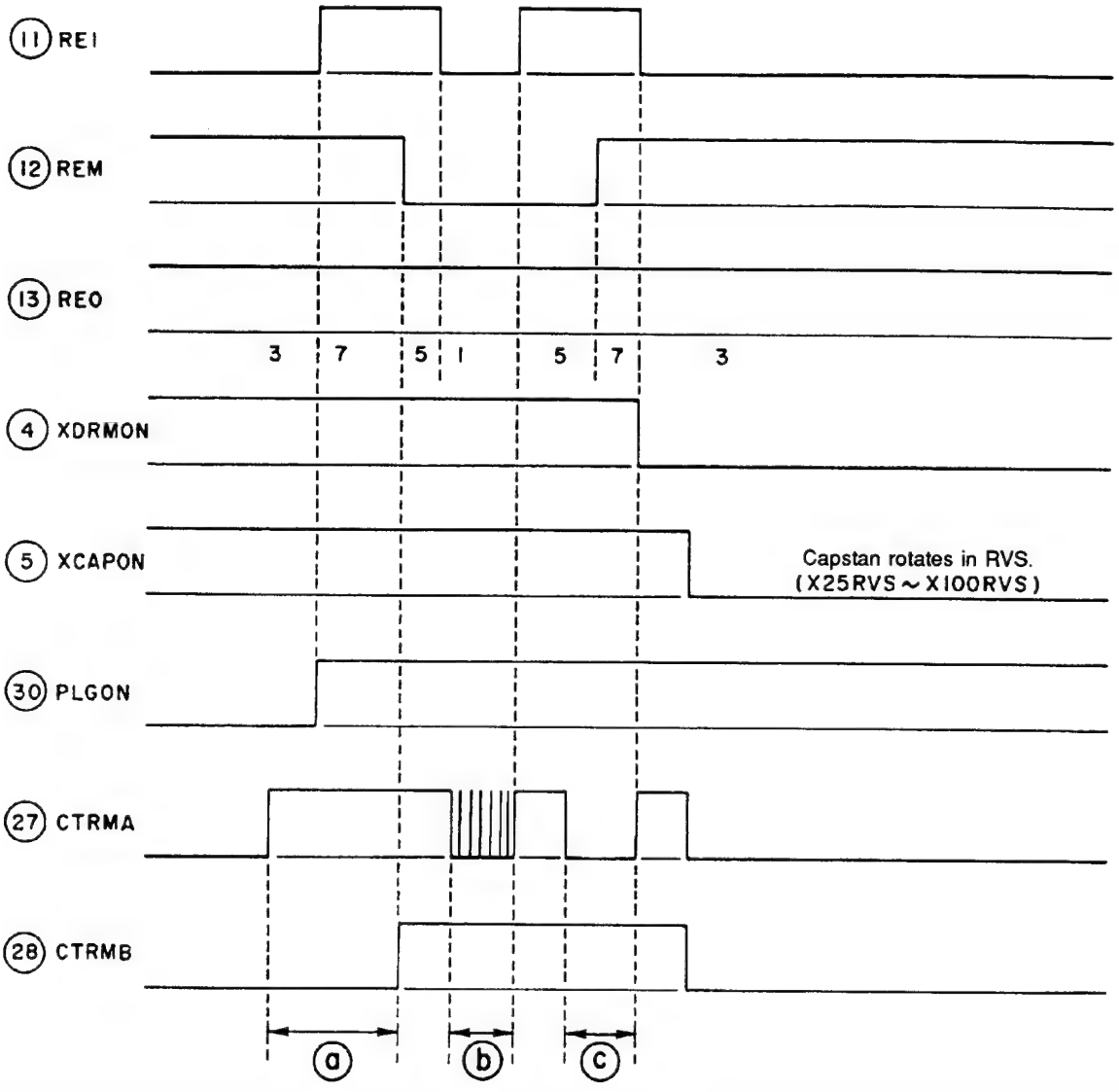
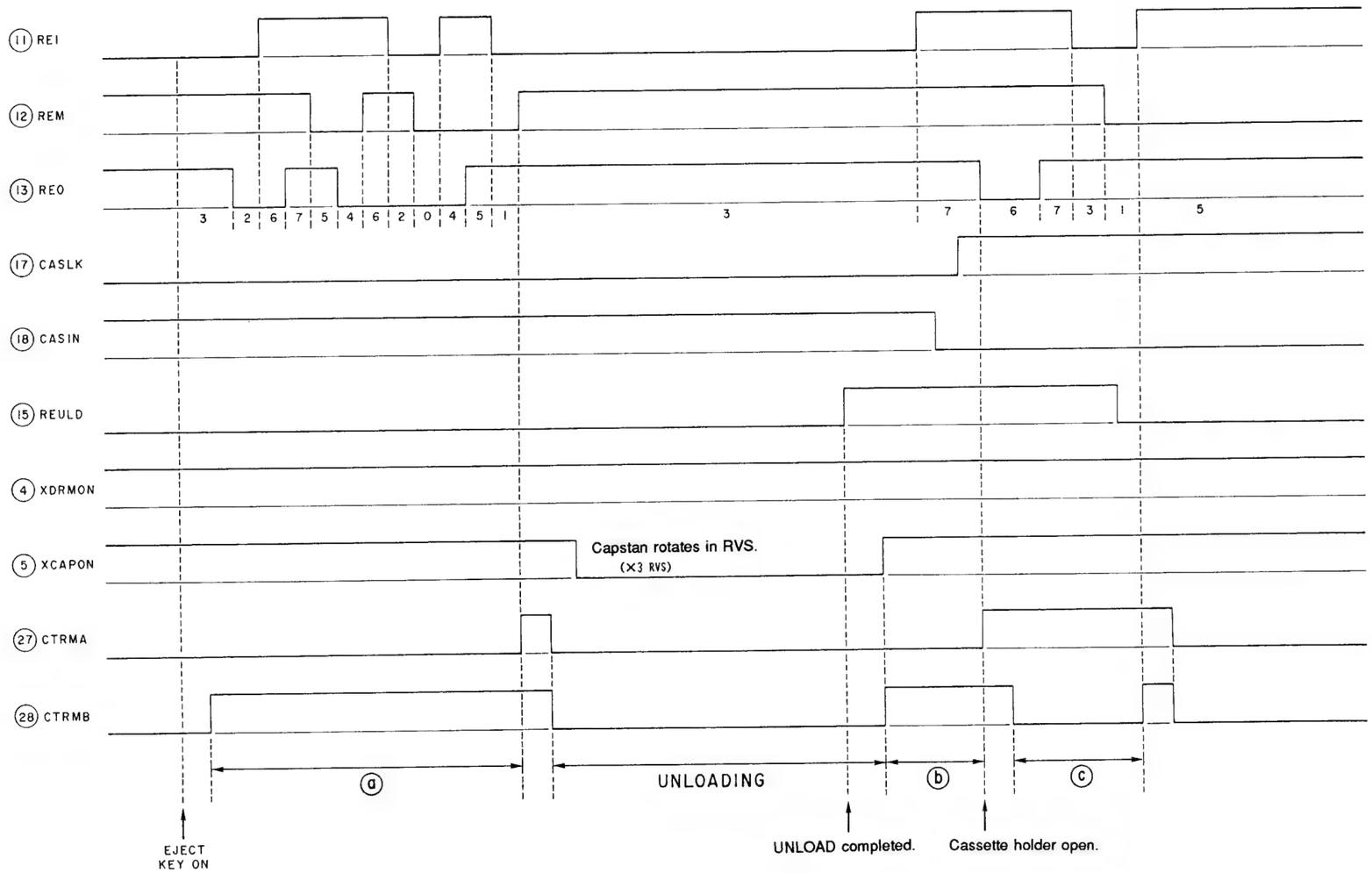


Figure 7-15. STOP → REW

7.6.7 STOP → EJECT

- **Operation when the EJECT button is pressed while in STOP**

Transition when EJECT is invoked while in the STOP mode is done by first moving the encoder to the UNLOAD position ((a)) and then, after that transition is finished, rotating the capstan motor in reverse at three times normal speed to unload the cassette. Then, the encoder is moved again to the EJECT position, after which time on operation is the same as in EJECT (see 7.6.2 EJECT). In this mode, therefore, the encoder performs the following operations: STOP → UNLOAD → EJECT → CASS IN.



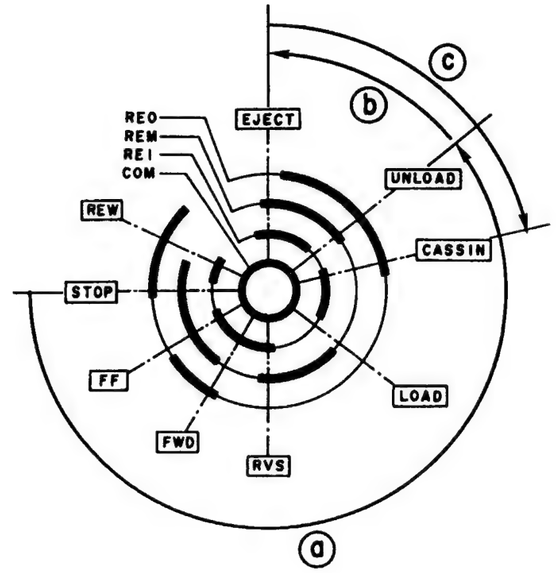
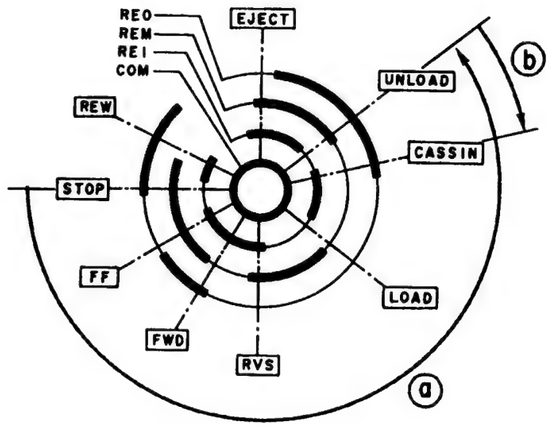


Figure 7-16. STOP → EJECT

7.6.8 STOP → POWER OFF

- **Operation when suddenly powered off while in STOP**

Transition when powered off while in the STOP mode is done by first moving the encoder to the UNLOAD position ((a)) and then, after that transition is finished, rotating the capstan motor in reverse at three times normal speed to unload the cassette. After that, the encoder is moved back to the CASS IN position to terminate its transition ((b)). The power supply is turned off immediately after transition to the CASS IN position is completed. In this mode, therefore, the encoder performs the following operations: STOP → UNLOAD → CASS IN.



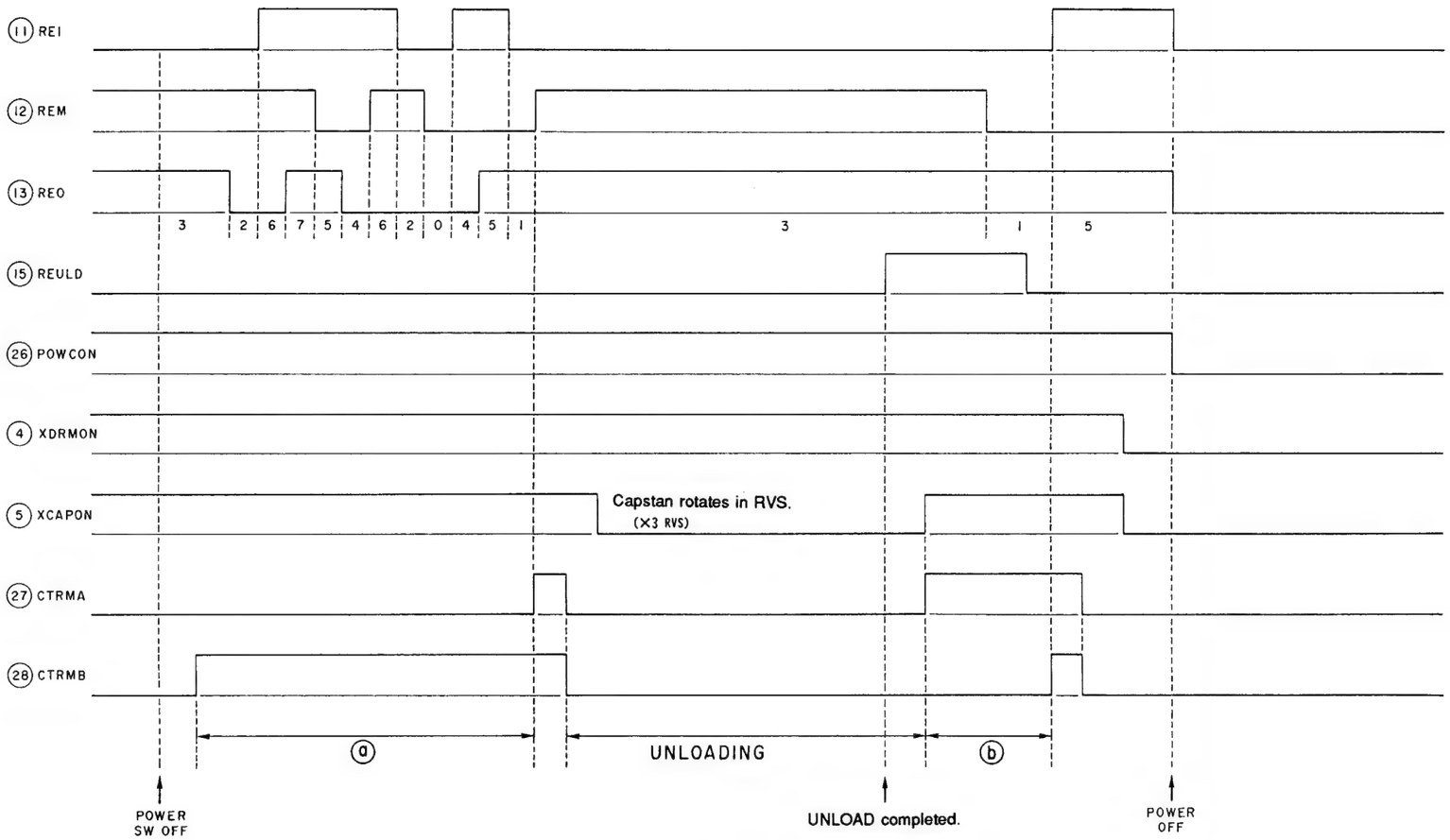
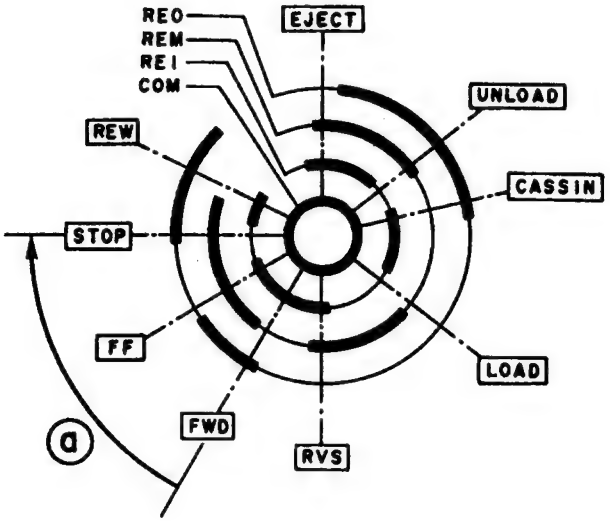


Figure 7-17. STOP → POWER OFF

7.6.9 FWD → STOP



Transition to the STOP mode is terminated by detection of the encoder's STOP position ((a)). The drum and the capstan motors are turned off with the same timing as the mode motor is turned on.

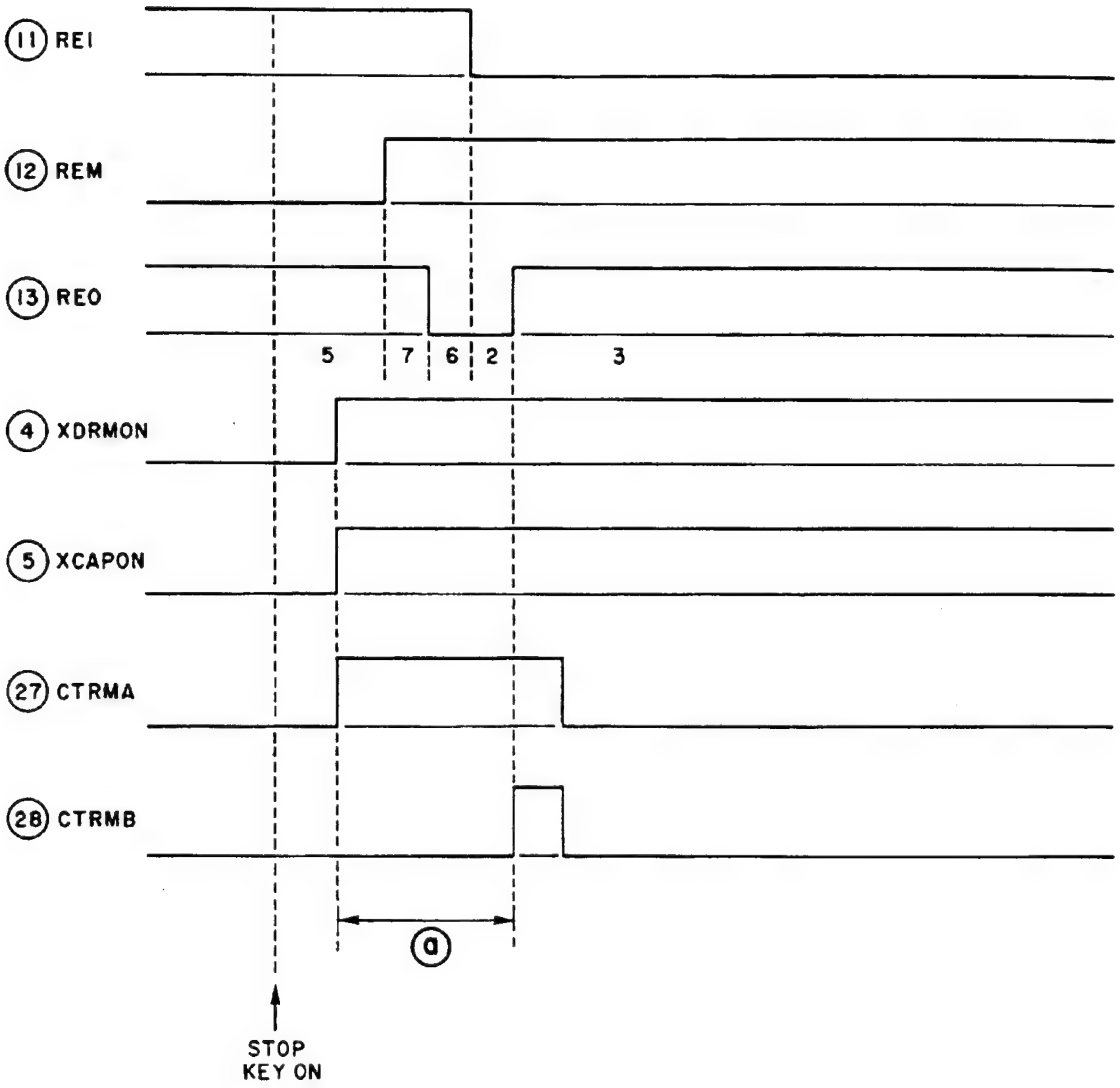
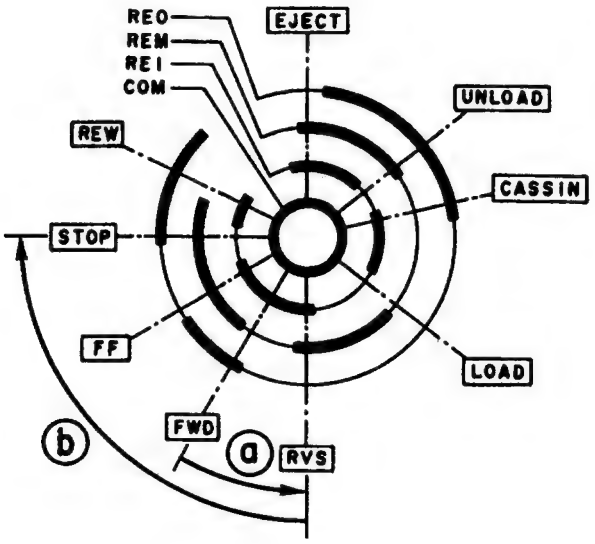


Figure 7-18. FWD → STOP

7.6.10 REC / REC PAUSE → STOP



Transition from REC or REC PAUSE to STOP occurs in such a way that the mecha mode is first moved to RVS ((a)) before moving to STOP to rewind the tape at normal speed for one second to ensure smooth connection between recordings. After this is done, the encoder is moved to the STOP position ((b)).

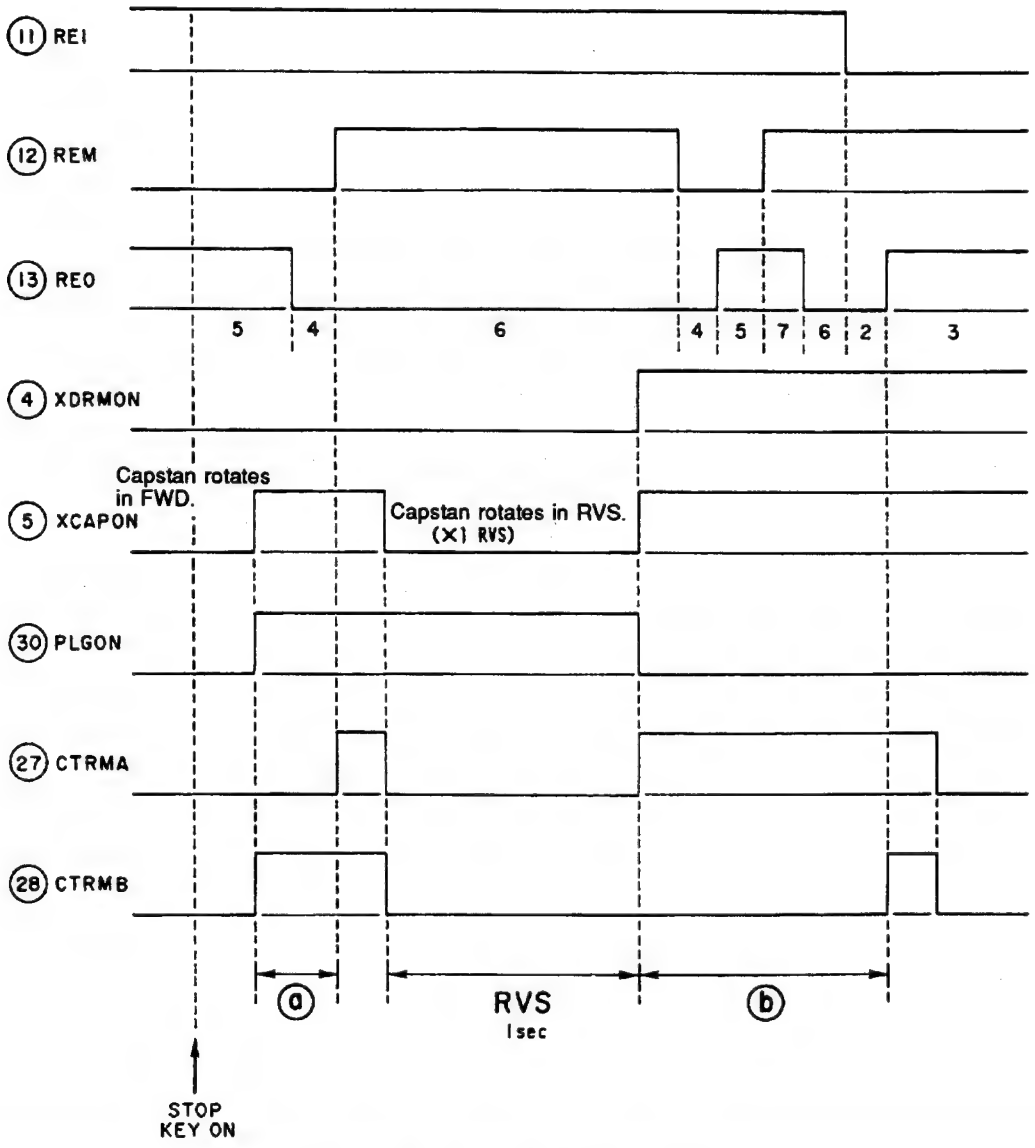
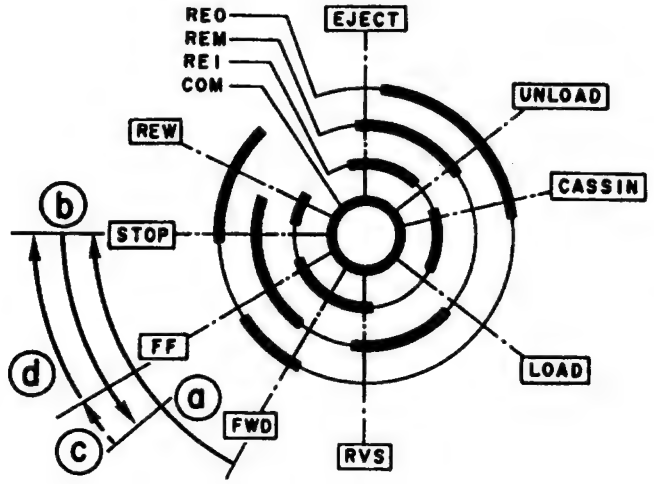


Figure 7-19. REC / REC PAUSE → STOP

7.6.11 FWD → X25 FWD (Fast CUE)



In this case, the encoder is temporarily moved to the STOP position ((a)) to apply the brakes mechanically before moving to FF ((b)) instead of making a direct transition from FWD to FF. Operation after that is the same as in transition from STOP to FF. (See 7.6.5 STOP → FF.)

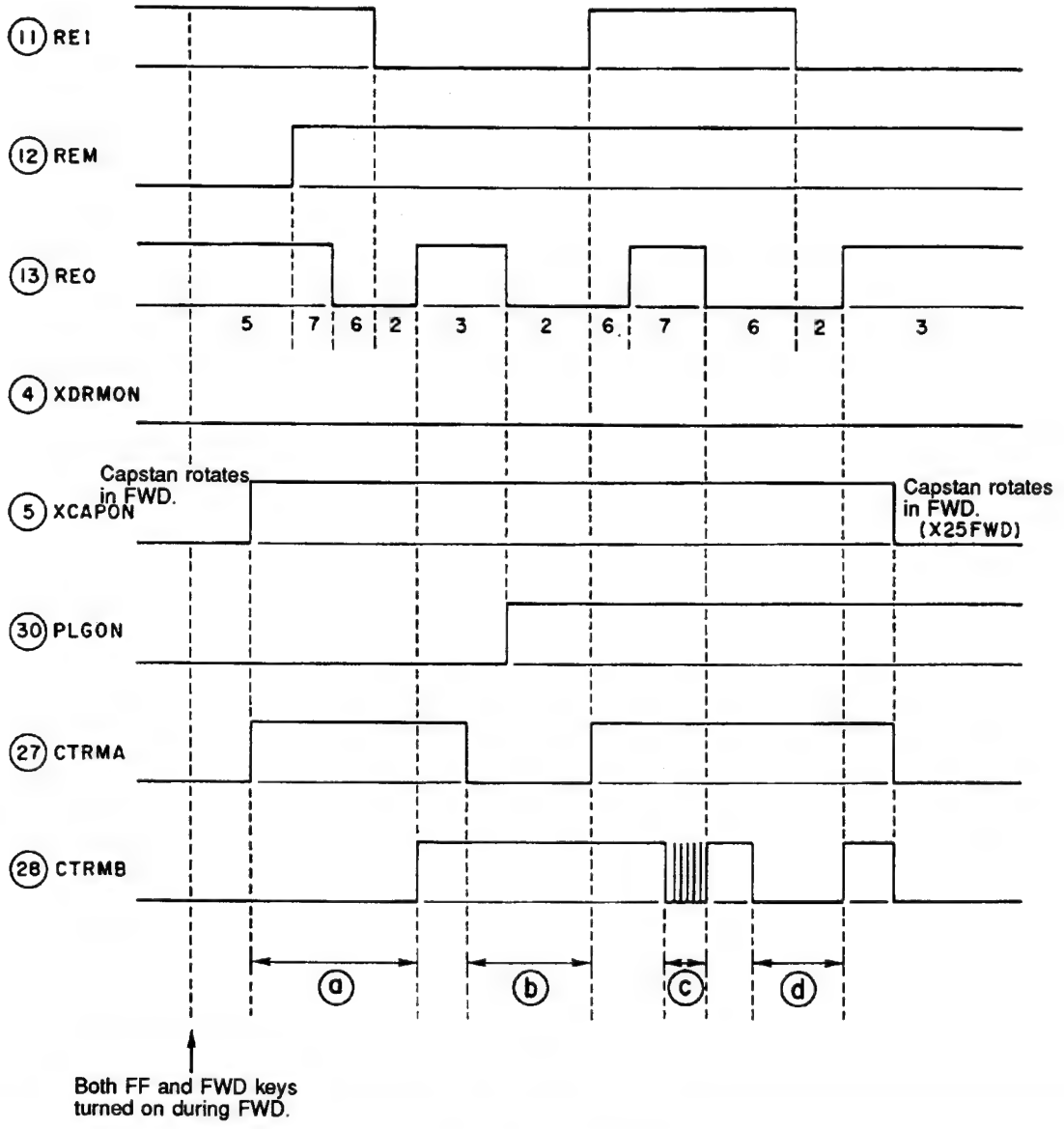
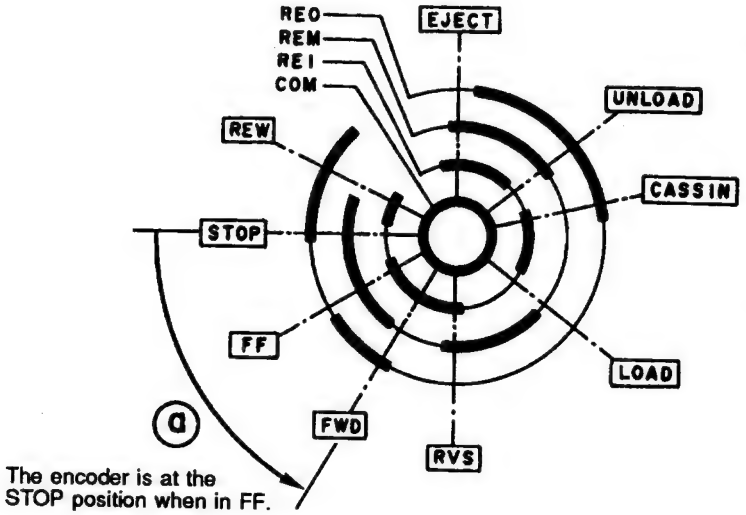


Figure 7-20. FWD → X25 FWD

7.6.12 FF / REW → FWD



When making transition from FF or REW to the FWD mode, mecha transition ((a)) is initiated after tape run is stopped (after the capstan motor is completely stopped) by applying the brakes instead of moving directly to the target mode. Here, the brakes are applied for only a predetermined time (200 ms), not by checking to see that the capstan motor is stopped.

FF → FWD

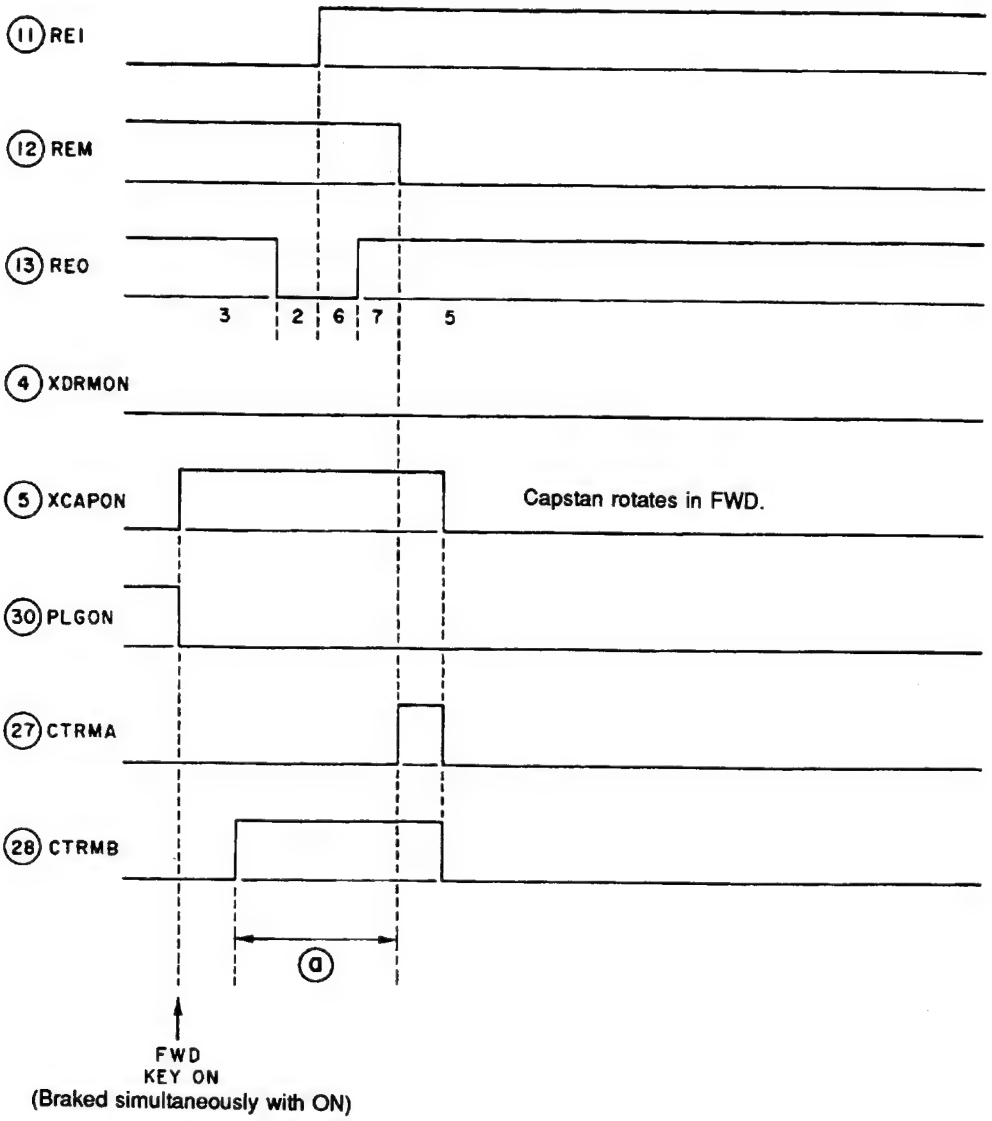


Figure 7-21. FF / REW → FWD

7.7 Automatic Writing of Start ID

When the start ID mode is set to AUTO, the start ID can be automatically written to tape during recording. This operation is, however, classified into "write by level sync" and "write upon REC start." Level sync is a method to determine whether the sound level exceeds a certain threshold, that is, whether the recording is with or without sound. For the TCD-D3, the threshold level is set to -50 dB. The start ID is automatically written when there is a sound after continuous silence for three seconds or more. To prevent pulse noise from being mistaken for sound, a match of multiple occurrences is used to determine the presence of sound. Note that the sound level is obtained from level meter data. For a write upon REC start, the start ID is written when sound is encountered first after REC is started from STOP or PAUSE.

The timing at which the start ID is written, is set to 0.5 seconds after the high-going transition of the RF or sound signal by considering after-recording.

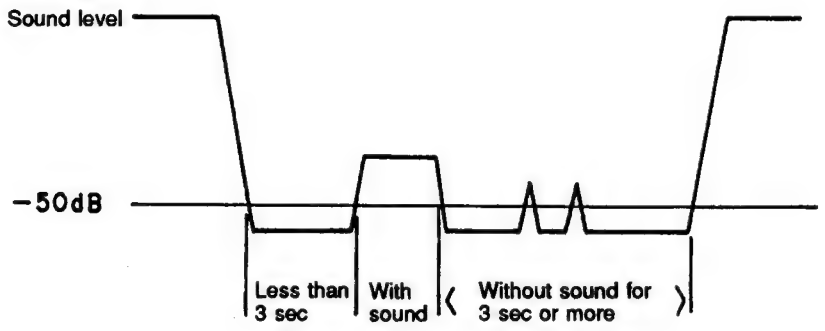


Figure 7-22. Level Sync

7.8 Tape TOP/END Processing

When broadly classified, this processing can be divided into two sessions of processing. One session of processing involves leader tape detection, that is, determining the LED drive and phototransistor signal. The other session of processing is for TAPE TOP tape feed processing including lead-in area processing. Figure 7-23 shows each sensor timing in leader tape detection.

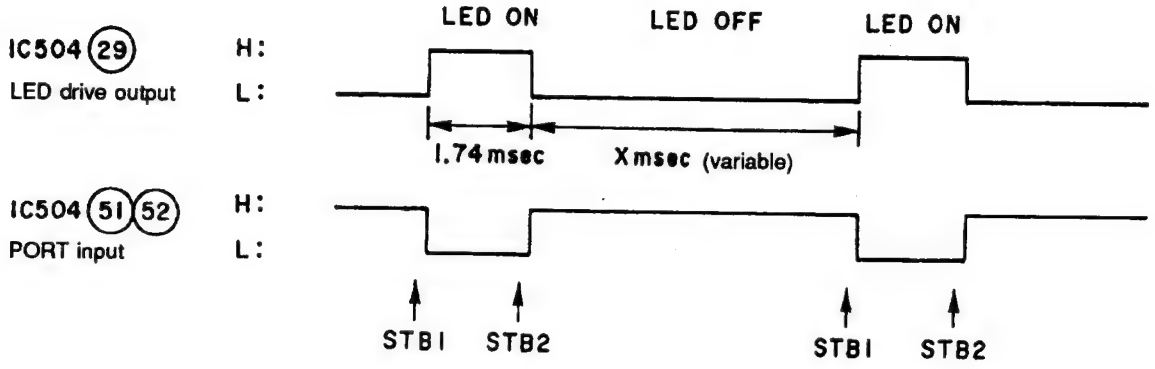


Figure 7-23. Each End Sensor Timing

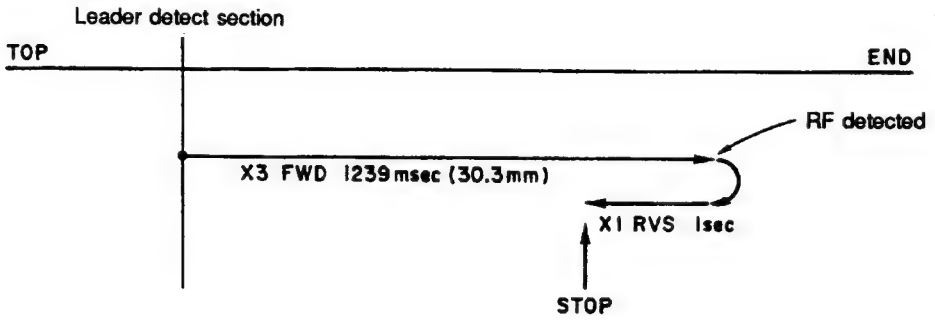
The end-detection LED drive waveform is such that the LED-on time is constant, always 1.74 ms, and that the LED-off time varies depending on the capstan speed (tape speed). The LED-off time is longest (i.e., 100.92 ms) when tape is run at normal speed and shortest (i.e., 1.74 ms) when tape is run in FF/REW. In the leader tape section, this LED light is transmitted to the phototransistor and the waveform is thereby reshaped and is returned to the microcomputer as an inverted signal of the LED drive waveform. The port input of this signal is determined by checking a High (STB1) immediately before the LED turns on and a Low (STB2) immediately before the LED turns off as a pair, so that when the same pattern is sampled twice, the microcomputer assumes it to be the leader tape section.

For the TAPE TOP tape feed and lead-in processing, determination of whether or not to write the lead-in area ("bb TOP" indicated interval) is done in such a way that when the top of tape is detected, the tape is forwarded at three times normal speed until a position about 30 mm from the joint of leader tape is reached. The presence of the RF signal is checked at this point in time; if not found, the tape is rewound a small distance and data indicating the lead-in area is written into the program number area of subcode.

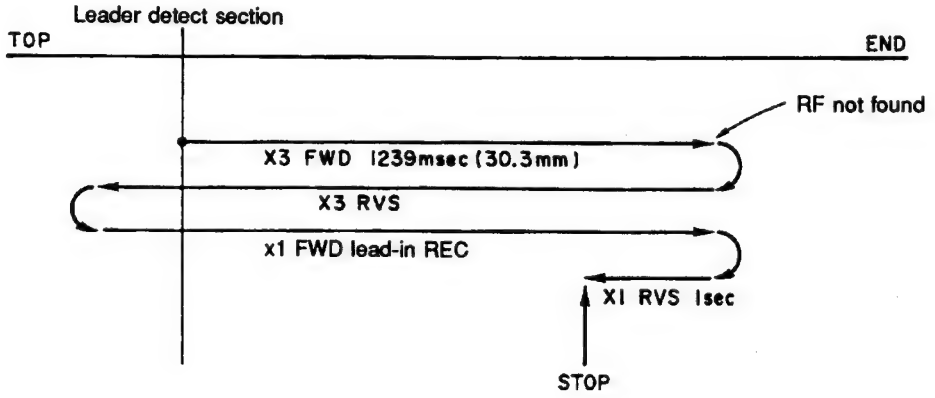
7.9 Capstan Speed and Sequence in Each Mode

1. Load and unload
   Load: x3 FWD
   Unload: x3 RVS

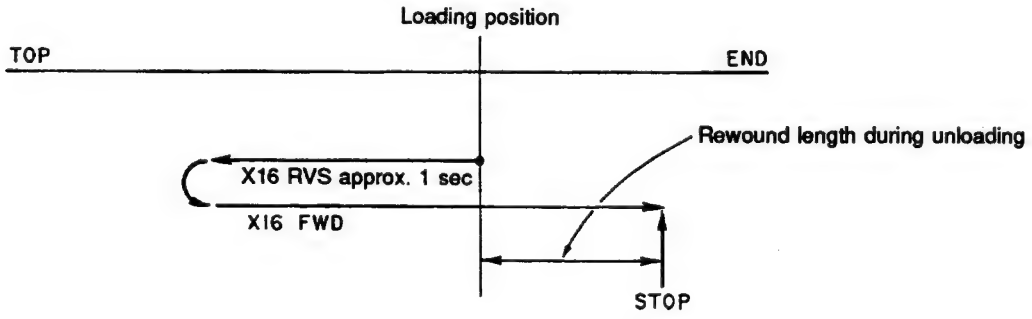
2. TAPE TOP processing
   (1) When lead-in area is not written



   (2) When lead-in area is written

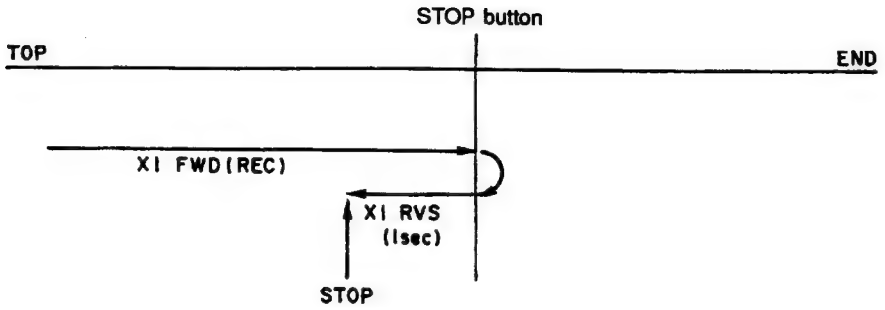


3. Initialize processing other than TAPE TOP

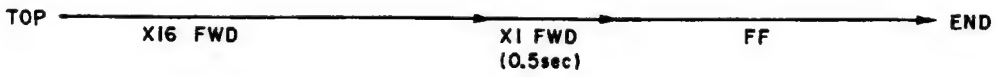


4. PLAY and REC
   In SP mode: x1 FWD
   In LP mode: x0.5 FWD

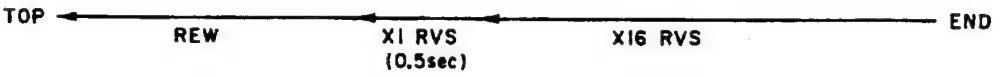
5. REC STOP



6. Measure (FF/REW)
   In FF: x16 FWD



   In REW: x16 RVS



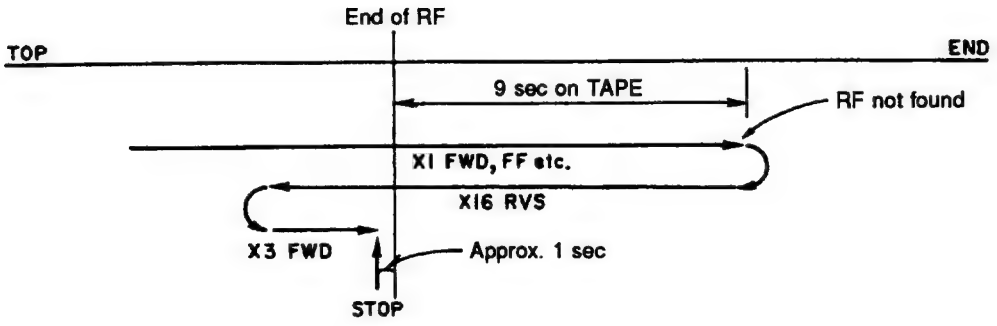
7. Slow CUE/REV
   In CUE: x3 FWD
   In REV: x3 RVS

8. Fast CUE/REV
   In CUE: x25 FWD
   In REV: x25 RVS

9. FF/REW
   FF: Target speed x25 FWD → When brought close to x25, the target is raised stepwise to x100 FWD.
   REW: Target speed x25 RVS → When brought close to x25, the target is raised stepwise to x100 RVS.

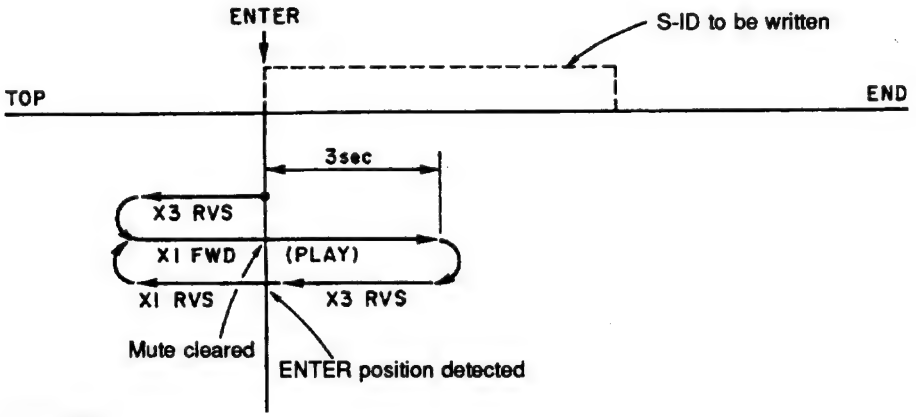
10. FF search / REW search
    - Startup in the same way as in FF/REW
    - For the after START ID is detected, see the separate sheet.

11. RF end processing

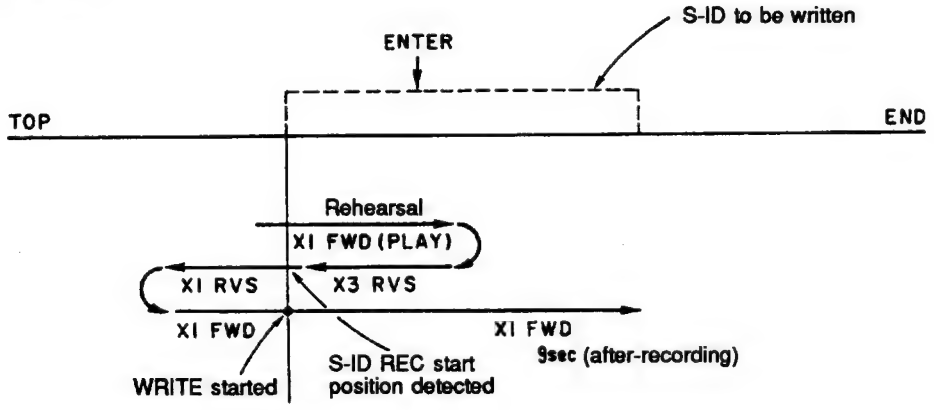


12. Writing START-ID in after-recording

(1) Rehearsal

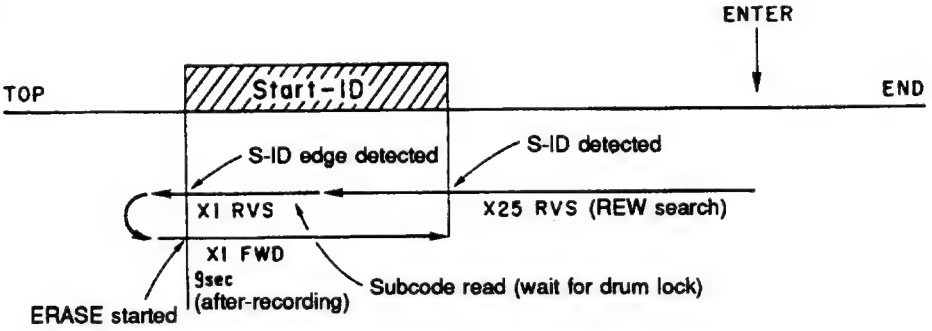


(2) WRITE

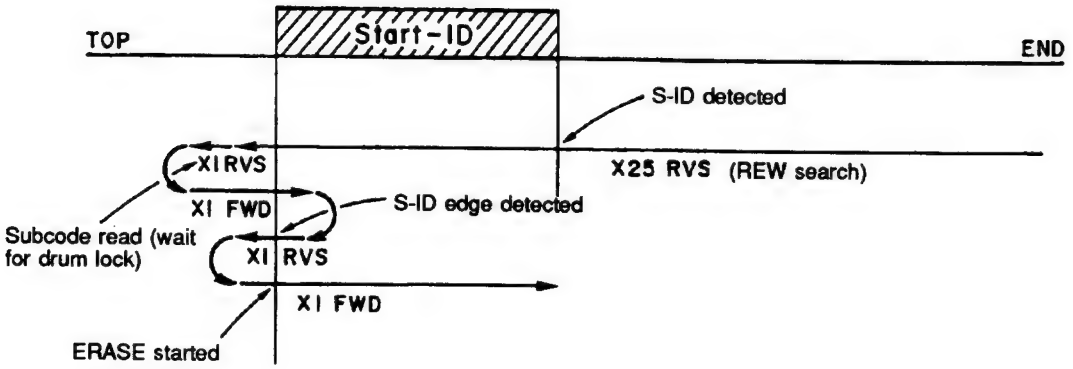


13. Erasing START-ID in after-recording

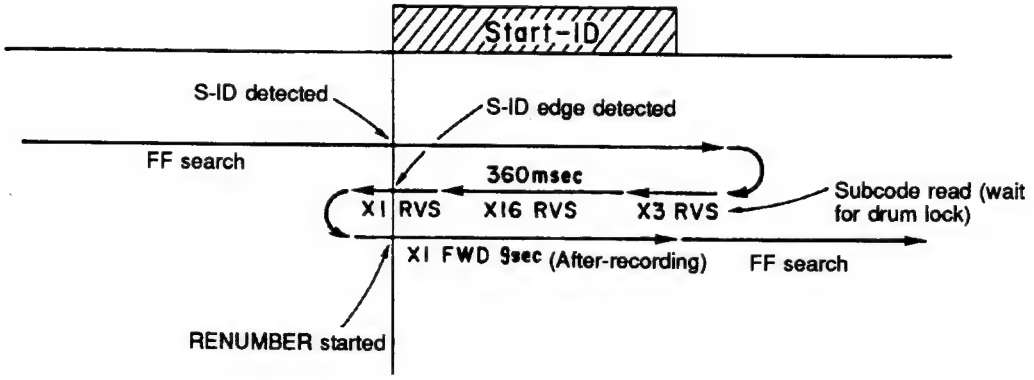
(1)



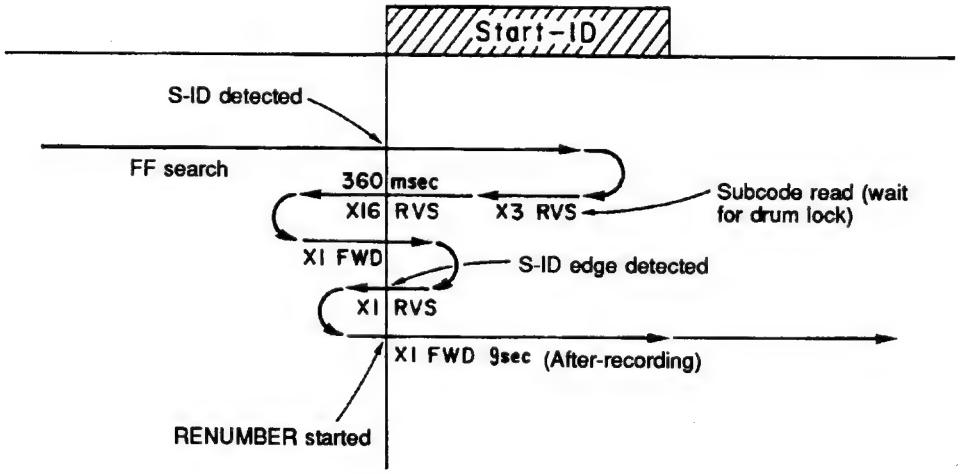
(2)



14. Renumbering START-ID in after-recording
* When ENTER is pressed, tape is first rewound to TAPE TOP and searched in FF.
(1)

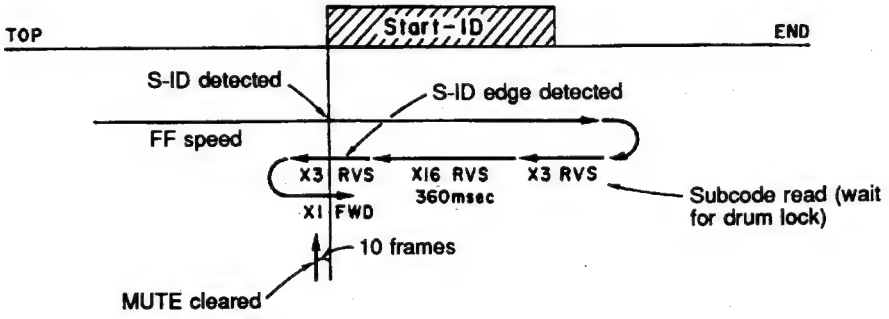


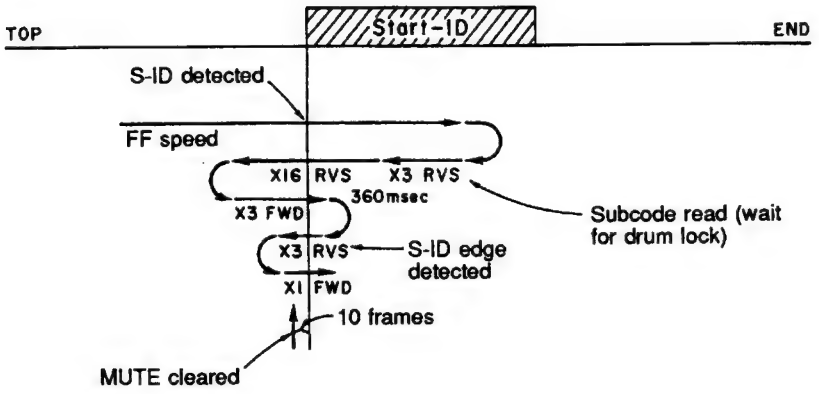
(2)



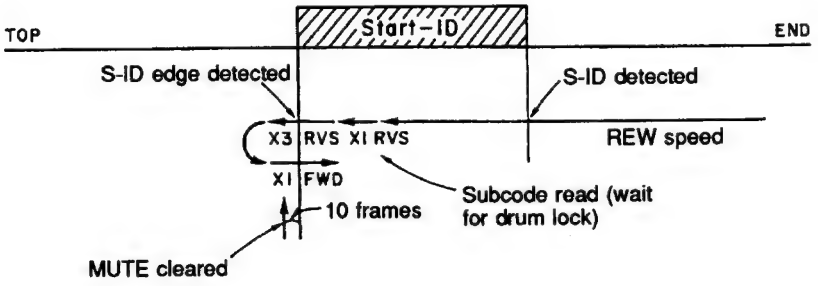
7.10 Sequence for Searching Beginning

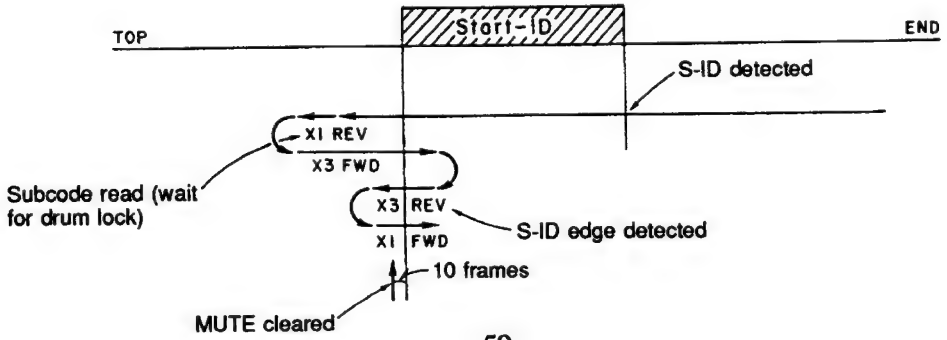
FF search





REW search





- During FF search, tape is rewound in x16 REV for a certain time and the subsequent sequence varies depending on whether the location is within or without the S-ID area.

- During REW search, tape is stopped upon detection of S-ID after being run at the REW speed (that is, when drum locked in x1 REV) and the subsequent sequence varies depending on whether the location is within or without the S-ID area.

- The reason why S-ID edge detection is done in x3 RVS is because if detected at 16 times normal speed, there will be a large error in the detected position.

- Although drum lock is waited for in x3 RVS during FF search, the same is done in x1 RVS during REW search. This is because if done in x3 RVS during REW search, tape may be run past the edge again before the drum locks.

7.11 Detection of Emergency

(1) During encoder position detection
Emergency is assumed if the desired position cannot be detected within five seconds after the mode motor started up.

(2) During loading/unloading
Emergency is assumed if loading/unloading transition is not completed within four seconds after it started (after the capstan motor started up).

(3) Takeup/supply reel emergency detection
Emergency is assumed if the reel FG is not input within a predetermined time, four seconds when in capstan motor startup or two seconds when in normal operation.

(4) Measure emergency detection
Emergency is assumed if measurement is not completed within 90 seconds (as indicated by the linear counter) after measurement started. If the tape speed changed during measurement, the emergency timer is reset and started again from that point in time.

(5) Drum emergency detection
Emergency is assumed if the drum motor is stopped and remains idle (as determined by the servo processing routine) two seconds after the drum motor started up.

(6) Capstan emergency detection
Emergency is assumed if the capstan motor is stopped and remains idle (as determined by the servo processing routine) four seconds after the capstan motor started up.

(7) End sensor emergency detection
This detection is done in only the test mode. Emergency is assumed if neither the top nor the end of tape can be detected within one second after the unit was placed in the test mode and end sensor check became possible.

(8) Drum lock emergency detection
This detection is done in only the test mode. Emergency is assumed if drum lock is released and remains off for 300 ms (as determined by the servo processing routine) seven seconds after the drum motor started up.

(9) Capstan lock emergency detection
This detection is done in only the test mode. Emergency is assumed if capstan lock is released and remains off for 300 ms (as determined by the servo processing routine) four seconds after the capstan motor started up.

8. Servo Circuit

8.1 Outline

The servo block consists of a capstan servo, ATF servo, reel servo, and a drum servo circuit as shown in Figure 8-1. The capstan servo controls the tape speed using the capstan FG to ensure that tape runs at a constant speed. The ATF servo provides tracking control using the ATF signal from the reproduction tracks so that the head always runs on the appropriate track correctly. The reel servo controls high- speed tape run as in FF and REW using the reel FG so that tape runs at a constant speed. The drum servo controls drum revolution to maintain it at a constant speed using PG and FG from the drum.

These servo circuits employ "software servo" which is known as an advanced, new method of servo control. As a result, external components and the locations to adjust have been greatly reduced.

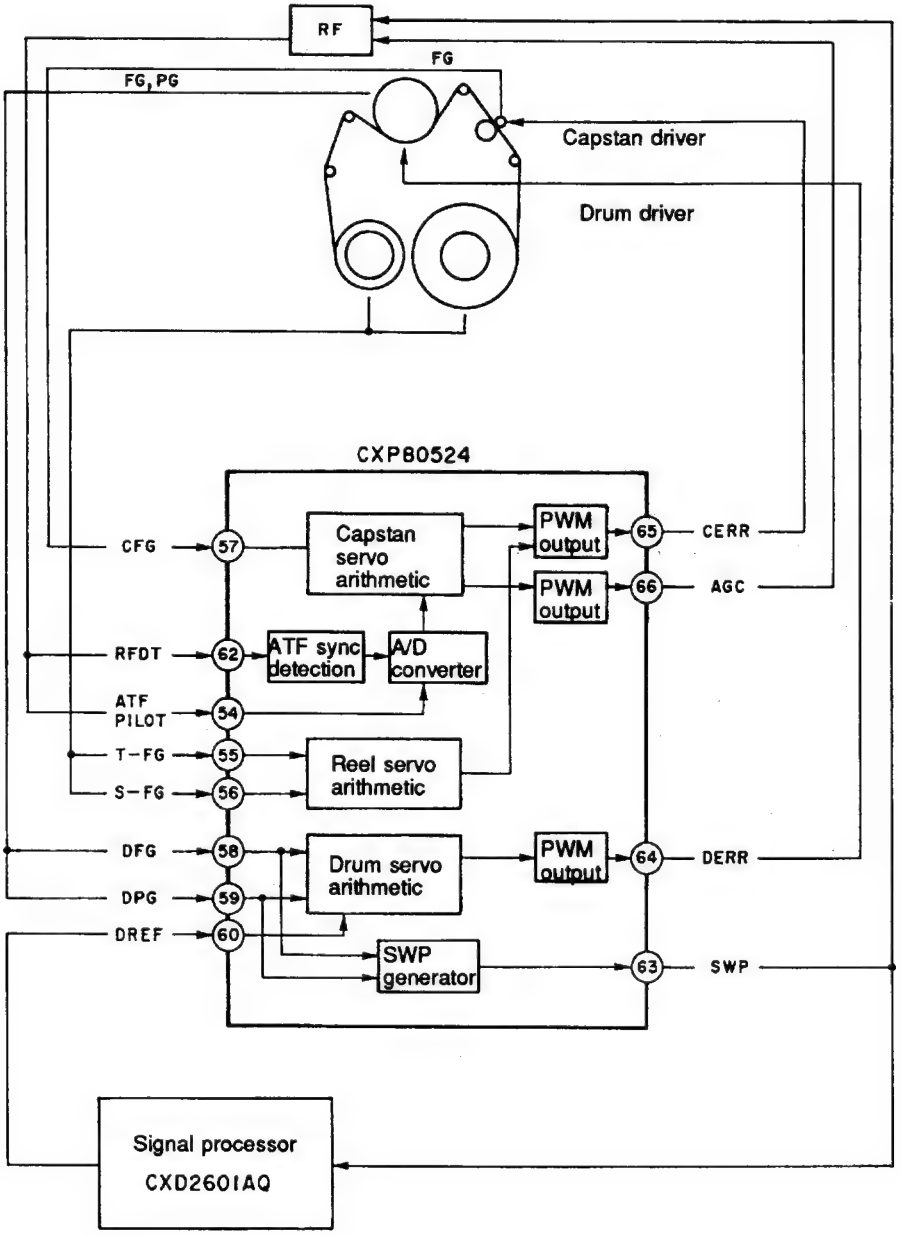


Figure 8-1. Schematic Diagram of Servo Block

The TCD-D3 uses a head drum in diameter of 15 mm. Table 8-1 lists drum revolution, transmission rate, and various other specifications of this type of head drum in comparison with conventional 30mm-diameter head drums. Comparing these two types of head drums, you see that drum revolution (N), drum reference (DREF), and tape feed speed (Vt) are the same in each mode. However, the 15mm head drum has half the tape- to-head relative speed of the 30mm head drum, so its transmission rate (R) is halved. Also note that drum revolution in the LP mode is 1,000 rpm during recording, but twice as fast (2,000 rpm) during playback. This ensures that the head reproduction output in the LP mode is almost the same as in the SP mode, and that the transmission rate during playback in the LP mode is also the same as in the SP mode. This provides numerous advantages including that there is no need to change the reproduction EQ circuit and PLL constants for each mode.

Note that although the head is not exactly on-track during playback, there is no problem with reproduction quality because the head reads the same track twice and the data which was read free-of-error is used as reproduction data. (For details, refer to 8.5.2 ATF Servo in LP Mode.) Also note that the head's trace angle during playback in the LP mode is slightly smaller relative to the track pattern on tape, so that data cannot be written to the designated subcode area when after-recording subcode. To solve this problem, the tape speed when after-recording subcode in the LP mode is increased to 8.15 mm/s (same as in the SP mode) to have the head trace angle matched with the track pattern for correct recording.

Table 8-1. Comparative Head Drum Specifications

		30mm-diameter drum (DTC-55ES)	15mm-diameter drum (TCD-D3)
REC	LP	N = 1000rpm	N = 1000rpm
		DREF = 50/3Hz	DREF = 50/3Hz
		Vt = 4.075mm/sec	Vt = 4.075mm/sec
		R = 4.704Mbps	R = 2.352Mbps
	SP	N = 2000rpm	N = 2000rpm
		DREF = 100/3Hz	DREF = 100/3Hz
		Vt = 8.150mm/sec	Vt = 8.150mm/sec
		R = 9.408Mbps	R = 4.704Mbps
PB	LP	N = 2000rpm	N = 2000rpm
		DREF = 50/3Hz	DREF = 50/3Hz
		Vt = 4.075mm/sec	Vt = 4.075mm/sec
		R = 9.408Mbps	R = 4.704Mbps
	SP	N = 2000rpm	N = 2000rpm
		DREF = 100/3Hz	DREF = 100/3Hz
		Vt = 8.150mm/sec	Vt = 8.150mm/sec
		R = 9.408Mbps	R = 4.704Mbps
Subcode after-recording	LP	DREF = 100/3Hz	DREF = 100/3Hz
		Vt = 8.150mm/sec	Vt = 8.150mm/sec
	SP	DREF m= 100/3Hz	DREF = 100/3Hz
		Vt = 8.150mm/sec	Vt = 8.150mm/sec

Note: LP = Long Play Mode
SP = Standard Play Mode
N = Drum Revolution
DREF = Drum Reference
Vt = Tape Feed
R = Transmission Rate

8.2 Sensor Amp (IC503 CXA1418N)

The CXA1418N contains five sensor amps (drum PG, drum FG, capstan FG, takeup reel FG, and supply reel FG of the R-DAT) integrated into a single chip.

Figure 8-2 shows its block diagram and pin assignment.

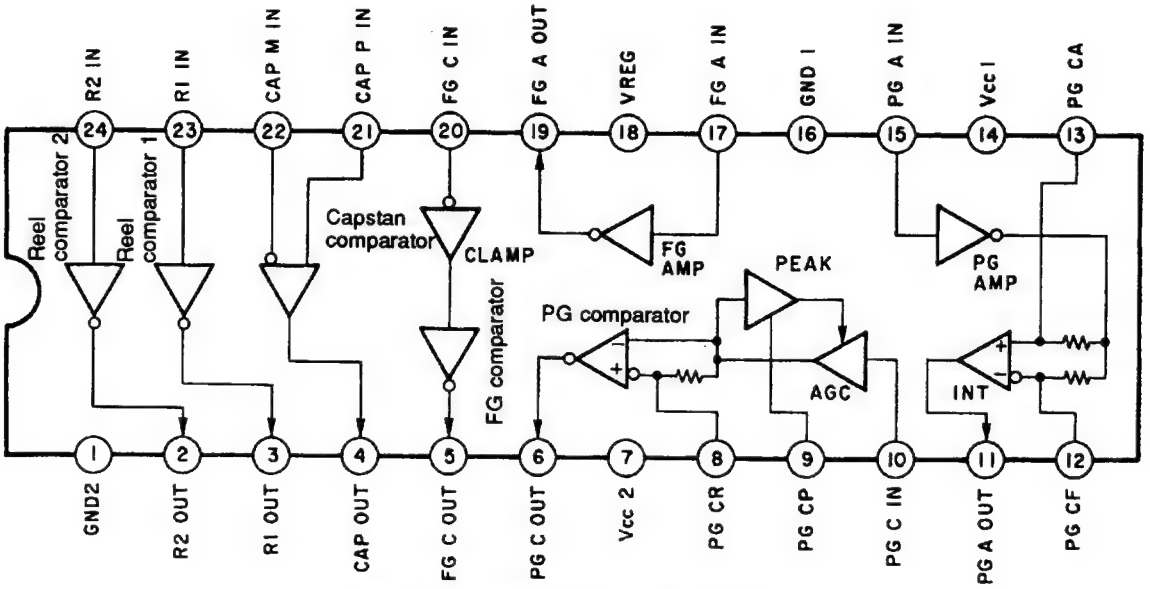


Figure 8-2. Block Diagram and Pin Assignment

Circuit Operation

- Drum PG amp
  The drum PG amp amplifies the very small output voltage of PG, ranging from several ten uVpp to several μVpp, to approximately 50 mVpp regardless of drum revolution by passing it through an integrator. This is a low-noise amp.
- Drum PG comparator
  The signal amplified to about 50 mVpp by the drum PG amp is input to this unit, and is amplified to about 600 mVpp after unevenness in the input level is eliminated by the AGC. This signal is processed by a comparator having a one-side hysteresis of 0-300 mV to extract only positive pulses which are output at 0-5 V.
- Drum FG amp
  The drum FG amp accepts as its input the drum FG sensor output of a 200Hz to 3.2kHz sine wave ranging in voltage from several hundred μVpp to about 10 mVpp and amplifies it approximately 63-fold. This is a low-noise amp.
- Drum FG comparator
  The signal amplified to about 40-640 mVpp by the drum FG amp is input to this unit, and is amplified to about 1.4 Vpp with its level limited by removing frequency components above 10 kHz. This signal is input to a comparator having a one-side hysteresis of 0-230 mV, and is output at 0-5 V.
- Capstan FG comparator
  This comparator receives as its input the differential signal of a magneto-resistance device and outputs it at 0-5 V.
- Reel FG comparator
  Having a threshold current of about 30 μA, this comparator receives as its input the current signal from the phototransistor. It contains two channels.
- Regulator
  A 3.2V regulator is provided as the internal reference power supply of the IC.

Pin description (CXA1418N)

Pin No.	Symbol	I/O	Pin description
1	GND 2	—	GND for 5-gang comparators
2	R2 OUT	O	Comparator output of reel FG 2
3	R1 OUT	O	Comparator output of reel FG 1
4	CAP OUT	O	Comparator output of capstan FG
5	FG C OUT	O	Comparator output of drum FG
6	PG C OUT	O	Comparator output of drum PG
7	Vcc 2	—	V_{CC} for 5-gang comparators
8	PG CR	I	Signal component smoothing capacitor input to generate the PG comparator reference voltage
9	PG CP	O	Peak hold capacitor output for the peak level detection of PG AGC
10	PG C IN	I	Input to AGC of drum PG
11	PG A OUT	O	Output of drum PG integrator
12	PG CF	I	Input of PG integrator feedback
13	PG CA	I	Smoothing capacitor input to generate PG integrator bias
14	Vcc 1	—	V_{CC} for devices other than the comparators
15	PG A IN	I	Input of drum PG signal
16	GND 1	—	GND for devices other than the comparators
17	FG A IN	I	Input of drum FG signal
18	VREG	—	Regulator output pin where smoothing capacitor is fitted
19	FG A OUT	O	Output of drum FG amp
20	FG C IN	I	Input of drum FG clamp
21	CAP P IN	I	Input of capstan FG signal
22	CAP M IN	I	
23	R1 IN	I	Input of reel FG 1
24	R2 IN	I	Input of reel FG 2

8.3 Drum Servo

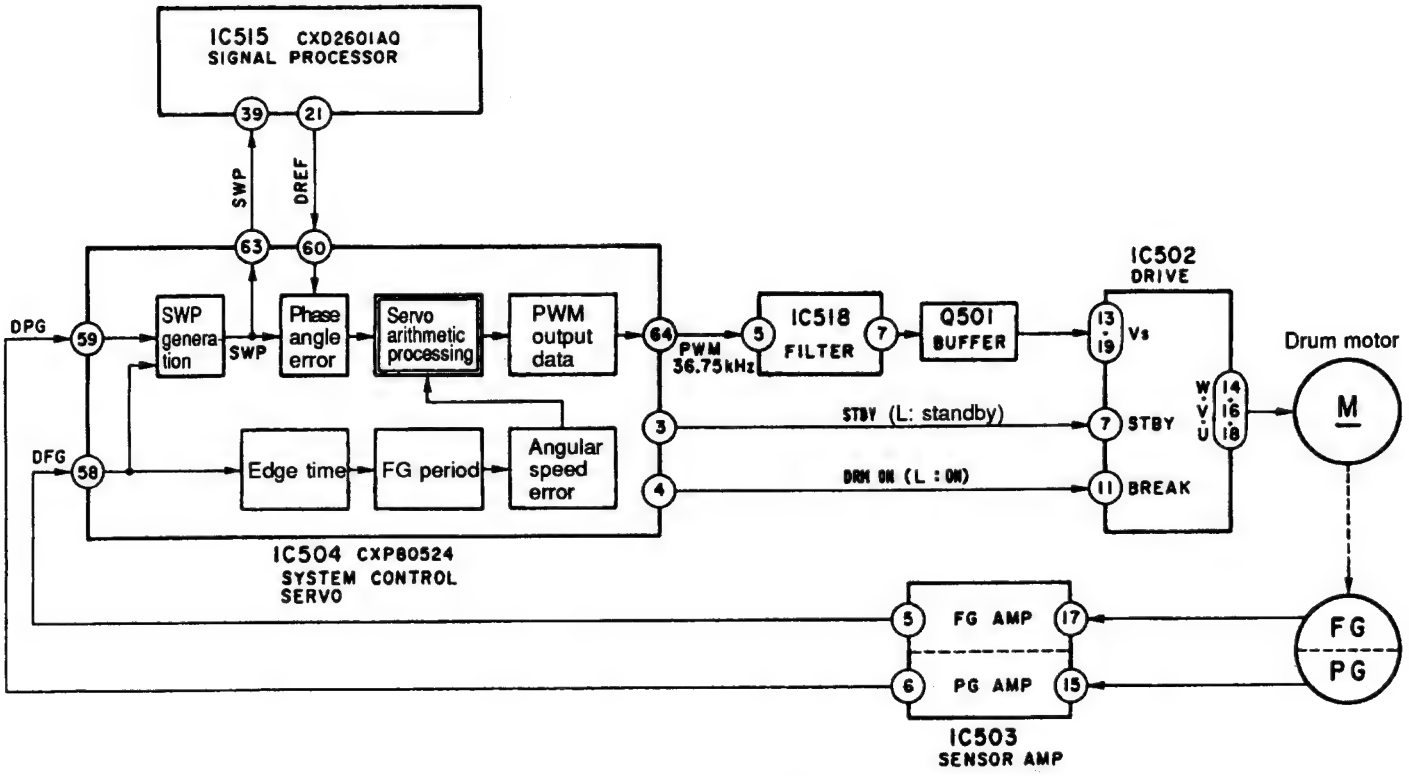


Figure 8-3. Drum Servo Block Diagram

The FG and PG signals from the drum motor are first reshaped of their waveforms by the sensor amp (IC503). Then, FG and PG are input to the CXP80524 (IC504) pin (58) and pin (59), respectively. In the CXP80524, the cycle time of FG is measured by a FG FRC (Free Running Counter) interrupt and the measured value is subtracted from the reference data. The resulting error data is output from pin (64) as a PWM output with the fundamental frequency of 36.75 kHz. On the other hand, PG is fed into the SWP generating circuit along with FG where SWP is generated with the timing shown in Figure 8-4. (The pulse width can be varied using VR501 to adjust the track write position. For details, refer to the description of SWP position adjustment in your service manual.) This SWP is phase-compared with DREF which is generated from the internal interleave reference signal of the CXD2601AQ signal processor, and the detected error component is added to the FG error data.

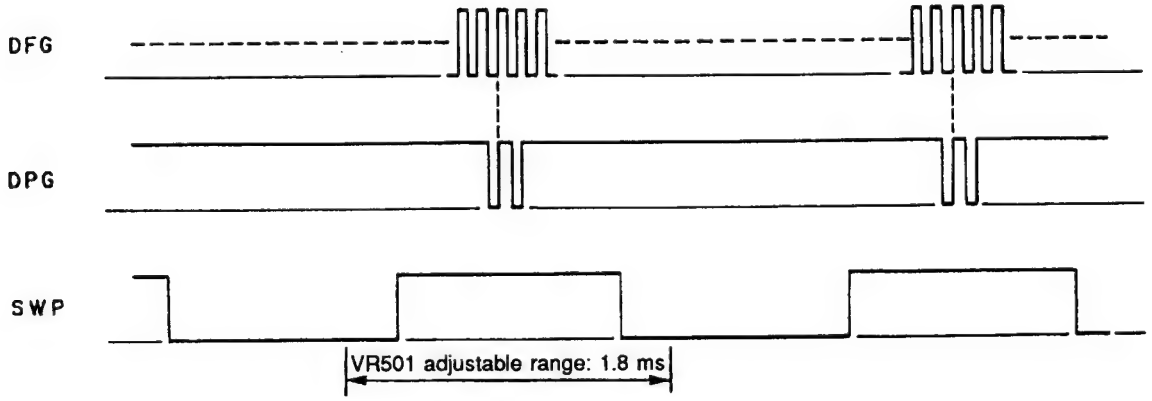


Figure 8-4. SWP Timing

The PWM error output from the CXP-80524 pin (64) is converted into analog voltage by a filter (IC518) and fed through a buffer (Q501) into the drum drive (IC502) to control the revolution of the drum motor.

Table 8-2. Each Signal Frequency during Drum Servo Lock

(Hz)	SP mode		LP mode	
	REC	PB	REC	PB
DREF	100/3	100/3	50/3	50/3
SWP	100/3	100/3	50/3	100/3
FG	800	800	400	800

When the drum servo is locked, drum revolution in the SP mode is 2,000 rpm during both recording and playback, and that in the LP mode is 1,000 rpm during recording and 2,000 rpm during playback. Table 8-2 shows the frequencies of DREF, SWP, and FG in these cases of operation. The signal timing in the SP mode is such that DREF and SWP are in-phase during both recording and playback as shown in Figure 8-5. The recording data (REDT) and the identification signal to indicate the ATF pilot area (PIPC) during recording are output from the signal processor CXD2601AQ (IC515) and the RF signal during playback is output from the RF module, both synchronously with DREF and SWP.

Signal timing in the LP mode is such that the period of each signal during recording is twice as long as the signal period in the SP mode, as shown in Figure 8-6, because drum revolution is half that of the SP mode. During playback, however, the periods of SWP and RF signals are the same as in the SP mode because drum revolution is the same 2,000 rpm as in the SP mode.

Note that the RF signal envelope during playback is not flat. This is due to the fact that drum revolution during recording and during playback are different. A and A' and B and B' respectively indicate the RF signal of the same track.

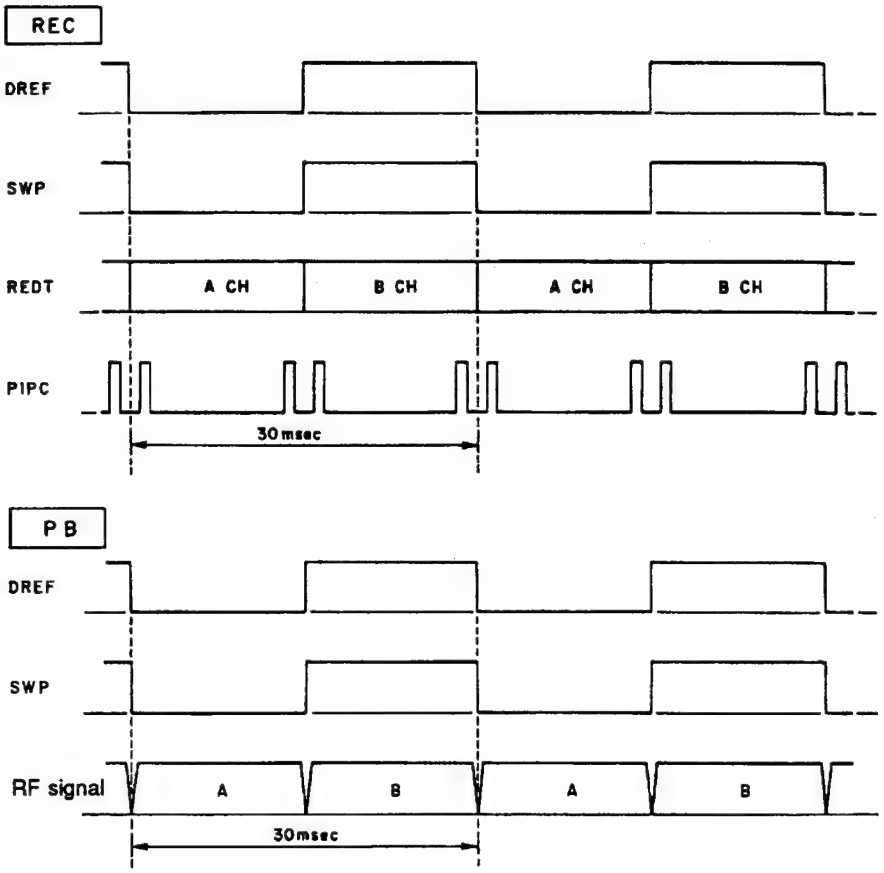


Figure 8-5. Signal Timing (SP Mode)

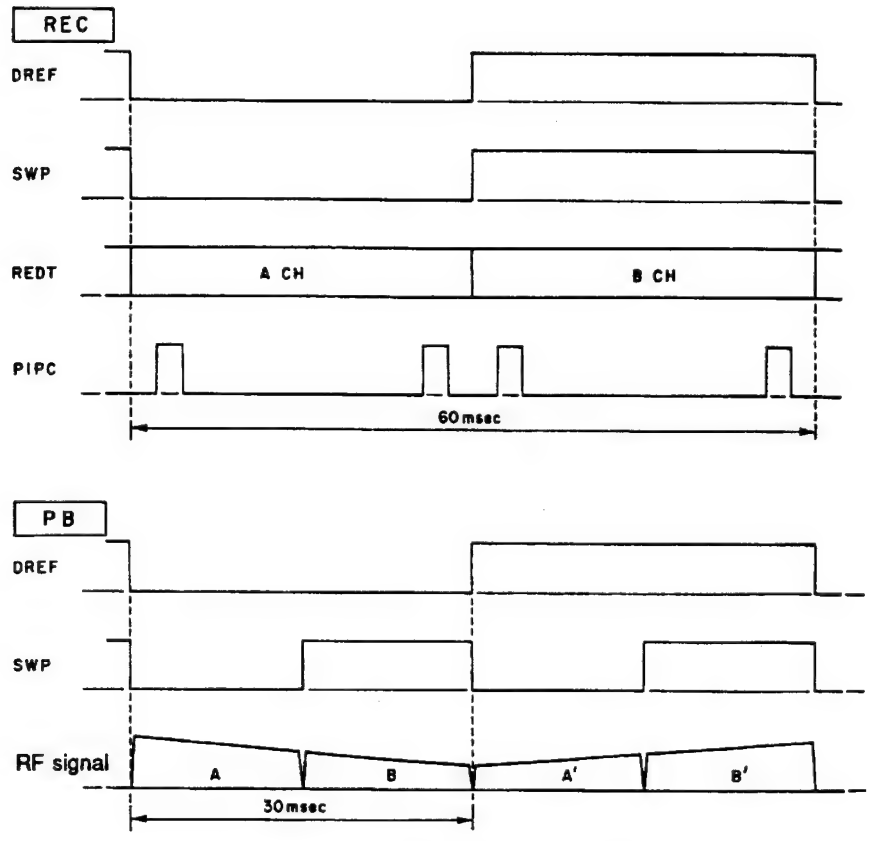


Figure 8-6. Signal Timing (LP Mode)

8.4 Capstan Servo

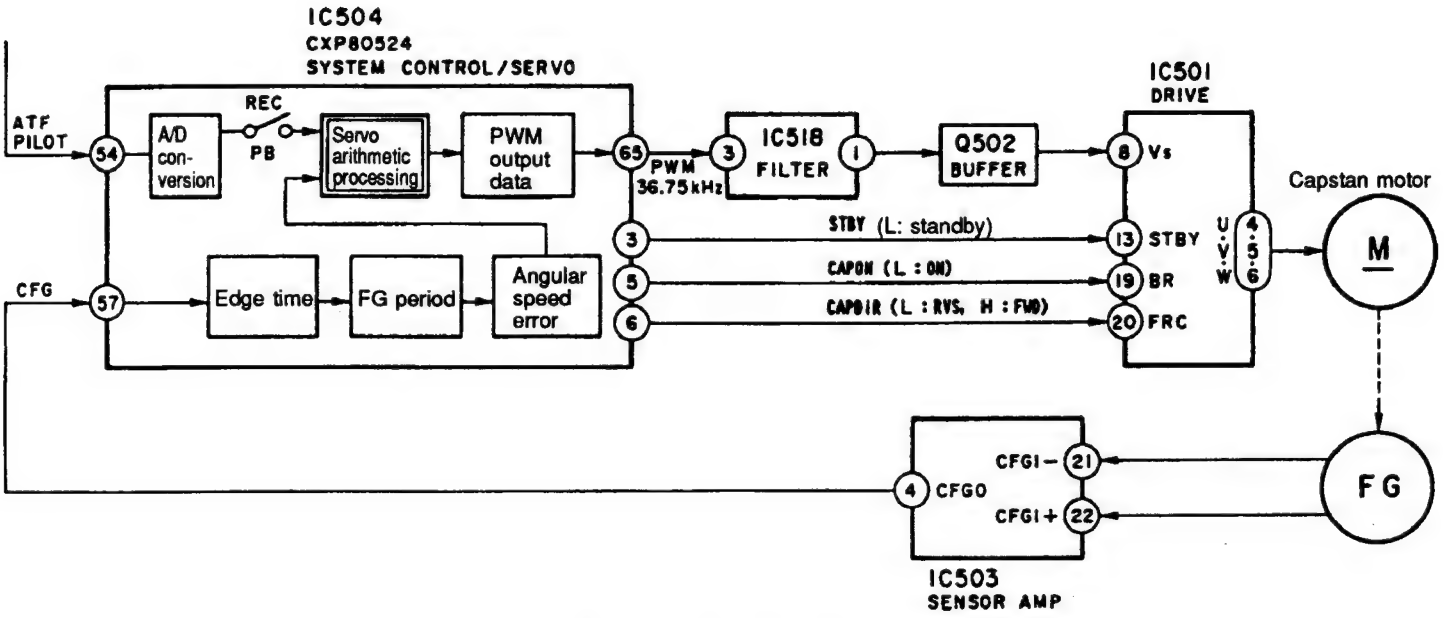


Figure 8-7. Capstan Servo Block Diagram

Table 8-3. Kinds of Capstan Speeds and Primary Uses

Speed	CFG(Hz)	Primary uses	Remarks
x 0.5	296	LP mode	• Capstan servo by CFG
x 1	592	SP mode	
x 1.5	888	Soft tape	
x 3	1,776	CUE/REV, LOAD/UNLOAD	
x 16	9,472	Measure mode	
x 25		Fast CUE/REV	• Reel servo by reel FG • Pinch roller not pressed against capstan
x 25 ≀ x 100		FF/FEW Search	

In addition to running tape at a constant speed along with the pintch roller, the capstan is used to load and unload tape and mechanism and drive the takeup and supply reel bases. Table 8-3 shows tape speeds in various modes. Of these, tape runs at speeds from x0.5 to x16 are controlled by capstan servo using CFG. High-speed runs for fast CUE/REV at x25 and for FF/REW and search at x25 to x100 are maintained at a constant speed by controlling the capstan motor revolution using FG from the takeup and supply reel bases. For this mechanical control, circuit operation is such that the FG output from the capstan motor is reshaped of its waveform by a sensor amp before being input to the CXP80524 (IC504) pin (57) as shown in Figure 8-7. In the CXP80524, the cycle time of FG is measured by a FG FRC (Free Running Counter) interrupt and the result is compared against the reference data as in the case of drum servo. The resulting error data is output from pin (65) as a PWM output with the fundamental frequency of 36.75 kHz.

During playback, the leak signal (ATF PILOT) from the adjacent tracks is A/D converted and the peak values of the leak signals from the preceding and following tracks are sampled with the timing of the sampling pulse to obtain error data by subtract calculation. The data is added to the FG error data for use in tracking control so that the head traces on-track correctly. During playback in the LP mode, furthermore, since the drum revolution is twice as fast (2,000 rpm) than in recording, the head traces one track two times at a different head-running angle than in recording. Therefore, tracking is controlled by software so that ATF servo is applied to only the just-on-track portion of tape. (For details, refer to 8.5.2 ATF Servo in LP Mode.)

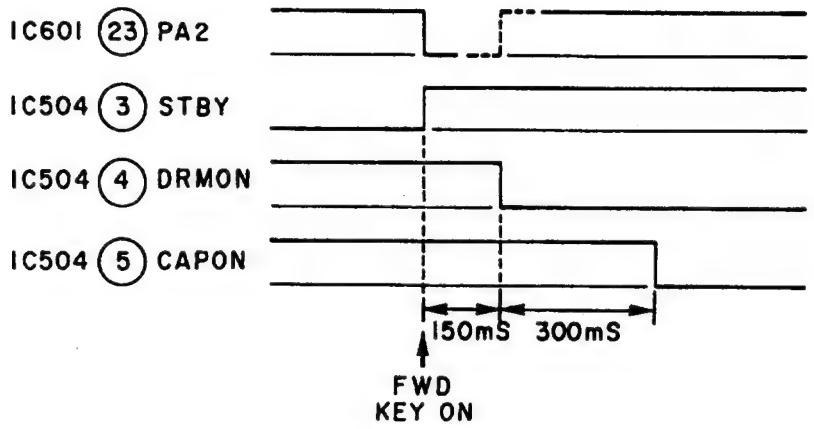


Figure 8-8. Timing When FWD Button Is Pressed

Figure 8-8 shows the timings of the standby ((3)), drum-on ((4)), and capstan-on ((5)) signals of the CXP80524 (IC504). When the FWD button is pressed, the signal on IC601 pin (23) goes Low, and STBY ((3)) goes High almost simultaneously with it, clearing the capstan drive (IC501) from its standby state. About 150 ms later, DRMON ((4)) is pulled Low to let the drum rotate, and CAPON ((5)) is forced Low 300 ms after that to cause the capstan motor to rotate. Note that CAPDIR on IC504 pin (6) is used to control the direction of the capstan motor rotation. When the signal is High, the capstan motor rotates in FWD.

8.5 ATF Servo

8.5.1 Configuration of Digital ATF Servo

The ATF servo was conventionally configured with analog servo. For the CXP80524, it is configured with digital ATF servo.

Therefore, this section first describes how traditional problems have been solved by using the digital ATF servo.

(1) Tracking offset caused by a capstan speed deviation (conventionally solved by adjustment)
→ The servo loop configuration was improved so that tracking offset does not occur even when there is a capstan speed deviation.

(2) Tracking offset caused by an unevenness in the sample- hold circuit DC offset
→ Need for the sample-hold circuit was eliminated, thanks to digital processing.

(3) Fluctuations in servo gain caused by an unevenness in the pilot signal reproduction level
→ Fluctuations in the pilot signal reproduction level were reduced by using an AGC servo.

(4) ATF servo configured with three chips (CXA1046, CXD1009, and CX20084)
→ The new ATF servo is configured with two chips (internal CXA1364 of RF module and CXP80524)

Figure 8-9 shows the configuration of the digital ATF servo.

The reproduction signal from the head is input to the head recording/playback amp (CXA1364) and is split into pilot signal envelope detection output (ATF PILOT) and reproduction data output (RFDT). The ATF PILOT signal is fed into the A/D converter which is built into the CXP80524, while the RFDT signal is input to the ATF sync detector which is also built into the CXP80524.

The ATF sync detector extracts the ATF sync signal from the RFDT signal to generate various sampling pulses (ATFS1, ATFS2, and ATFS3) which are used to detect the PILOT signal. These sampling pulses are input to the A/D converter, as well as to the FIFO control circuit used to store the A/D conversion result in memory. In this way, the A/D conversion of the PILOT signal is automatically executed by hardware.

The A/D-converted data of the PILOT signal is used to detect tracking and AGC errors for digital filter arithmetic processing. After this arithmetic processing, the tracking control data is presented to the PWM output circuit where it is converted into capstan motor control voltage. Similarly, the arithmetic-processed AGC control data is forwarded to the PWM output circuit where it is converted into gain control voltage for the gain control amp (GCA) of the CXA1364. (For details, refer to 8.5.3 ATF AGC.)

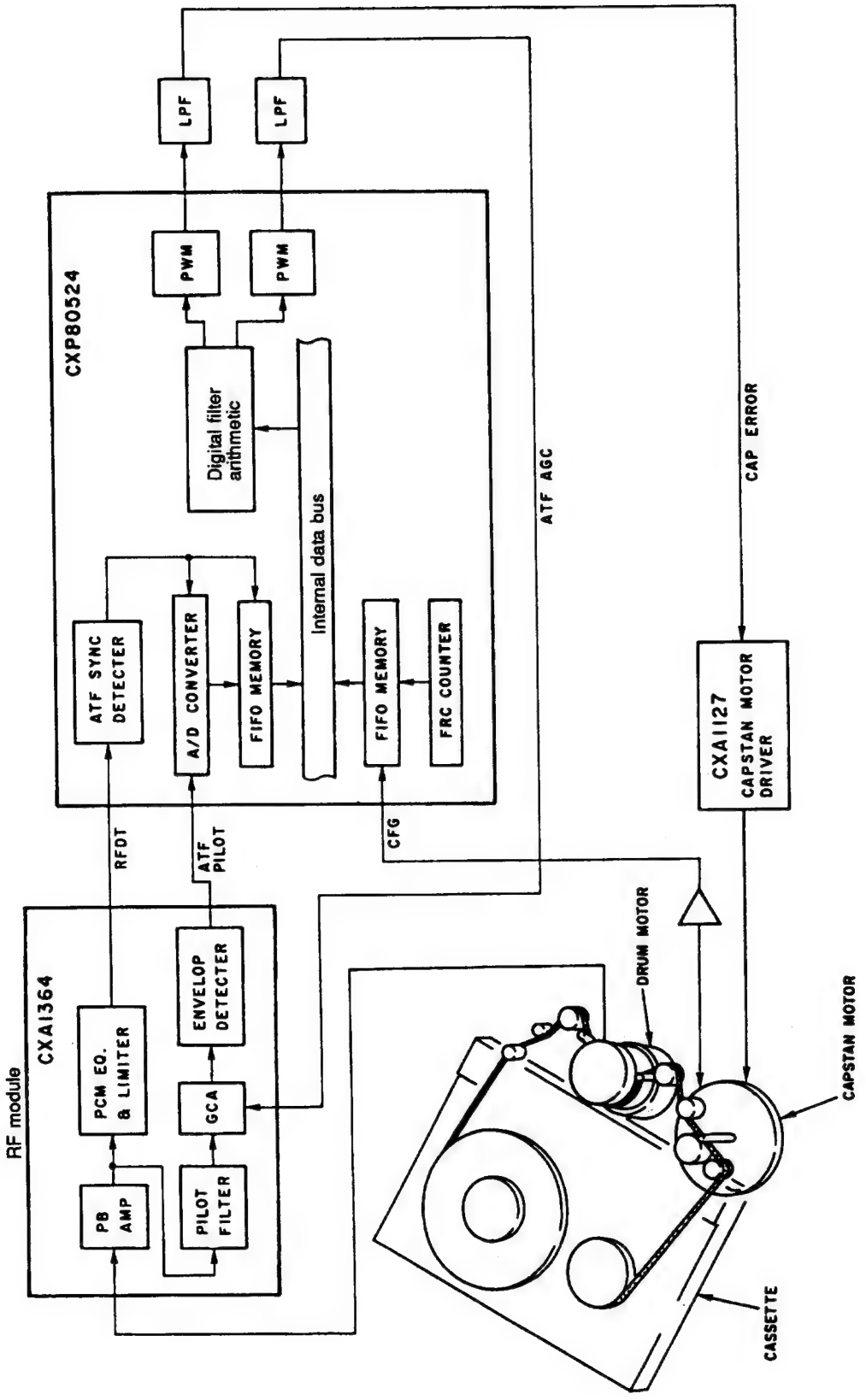


Figure 8-9. Configuration of Digital AFT Servo

8.5.2 ATF Servo in LP Mode

This section describes the LP mode ATF servo which was made possible for the first time by using the second-generation DAT LSI.

In the LP mode, the drum is rotated at 2,000 rpm to ensure that the tape-to-head relative speed during playback is the same as in the SP mode (that is, to produce the same head reproduction output as in the SP mode). Since the tape speed in the LP mode is half that of the SP mode, the head traces each track two times with a different head-running angle than the REC angle (recorded inclination angle of track) during playback in the LP mode. In this case, the signal processor LSI (CXD2601AQ) selects one from these two reproduction data that has no error after error correction when it generates audio reproduction signal. Thus, when the head traces the same track twice, you only need to be able to reproduce one of the two data.

To obtain reproduction data with the smallest error rate possible while tracing the same track twice as such, it is only necessary to control the head tracing locus so that the head reproduction output from either tracing locus is maximum for both heads A and B at the same level, as shown in Figure 8-10 (for portable DAT). Control is also applied using the interleave period of the signal processor LSI (CXD2601AQ) to ensure that the maximum head reproduction output within one DREF cycle is obtained when reproducing the track of the same frame address, for both heads A and B.

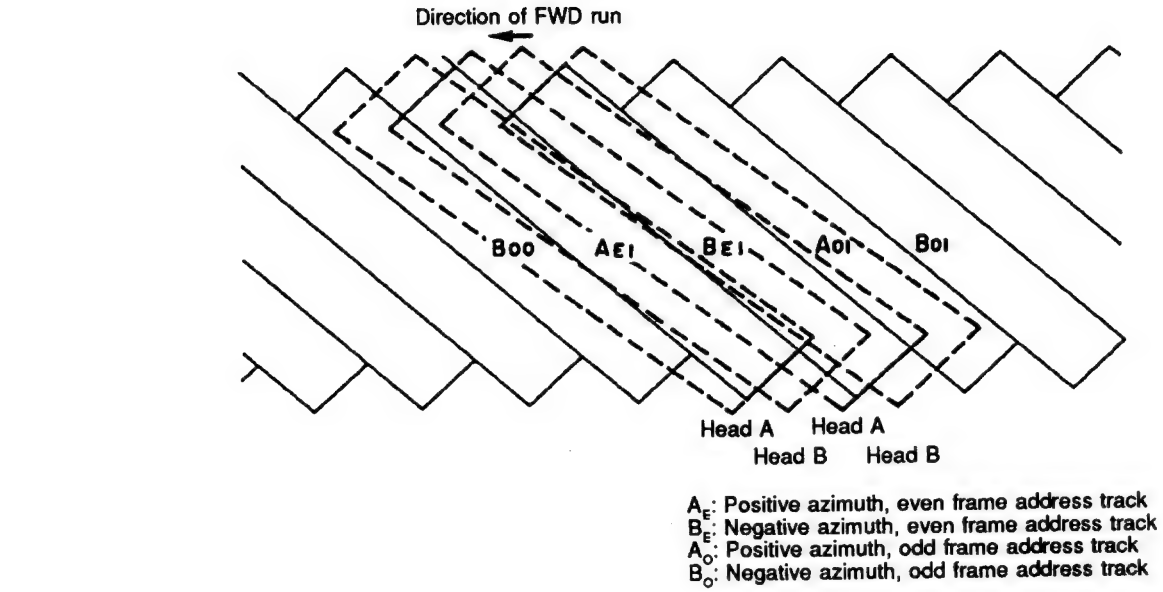
Now the following describes the tracking method employed to accomplish the tracing locus in Figure 8-10.

The head tracing loci (a) and (d) in Figure 8-10 are almost just-on-track while (b) and (c) are severely off-track. If all ATF sync signals are detected and ATF servo applied in such a state, the tracking position may drift from the head run state in Figure 8-10.

To attain the head tracing locus in Figure 8-10, therefore, a technique is employed so that ATF sync signal detection is disabled when the head is tracing (b) and (c), and ATF servo is applied using only the tracking error detected when the head has traced (a) and (d). Note that in this scheme, ATF sync detection is turned on and off by controlling the ATF window (ATFW) signal of the ATF sync detector via software, and that the head traces (a) and (d) are determined by checking the SWP and DREF signal polarities.

8.5.3 ATF AGC

Automatic adjustment of RF amp gain (called ATF AGC) is applied to prevent erroneous ATF operation due to differences in recording current on the tape to be reproduced. ATF AGC is based on a principle that the sum of leak signals from two adjacent tracks is always constant regardless of whether tracking drifts from the right position. Therefore, the gain control amp (GCA) in the RF amp is DC-controlled to ensure that the sum is within the predetermined value. The ATF pilot area is located at two positions on each track, and which area to be used is determined by software depending on operation modes (e.g., LP and SP).



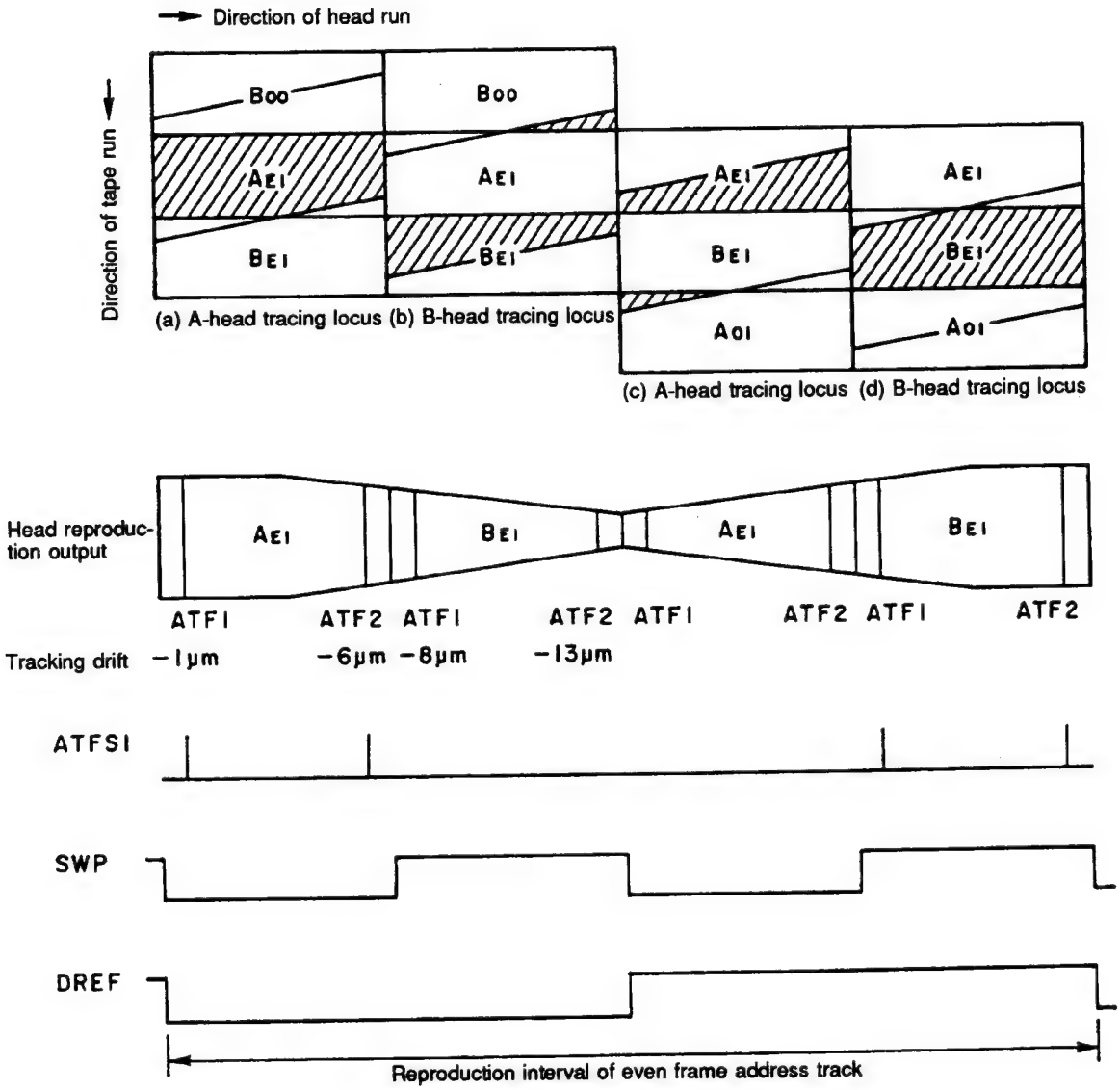


Figure 8-10. Head Tracing Locus in LP Mode

8.6 Other Servo

8.6.1 Search Servo

Search servo is comprised of constant tape speed (about 100 times normal speed) control based on a reel FG interrupt and drum servo to maintain a constant tape-to-head relative speed. The reel servo is applied to maintain a constant speed regardless of tape length by calculating the current speed from the FG periods of both reels. In this case, however, the tape speed is not raised to 100 times normal speed immediately after startup. A target is set at 25 times normal speed first and when the tape speed is within a certain range relative to it, the target value is incremented one by one at certain time intervals until 100 times normal speed is reached. (See Figure 8-11.) Then, drum servo is applied to ensure that the head can read the signal best at that speed.

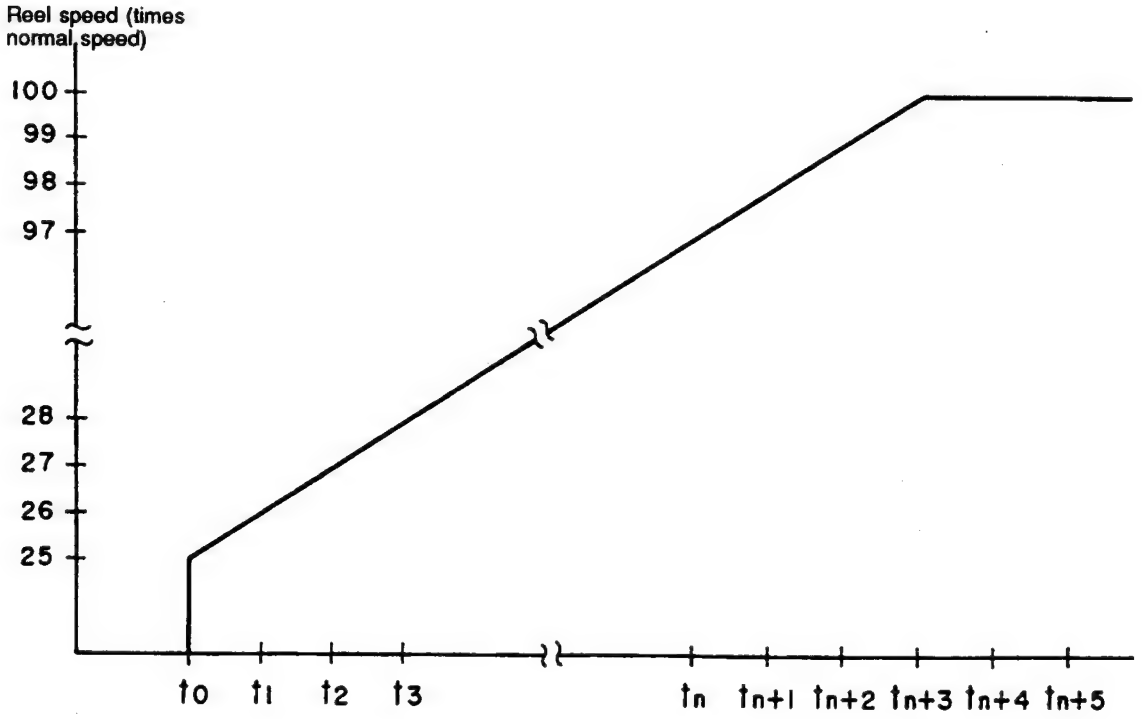
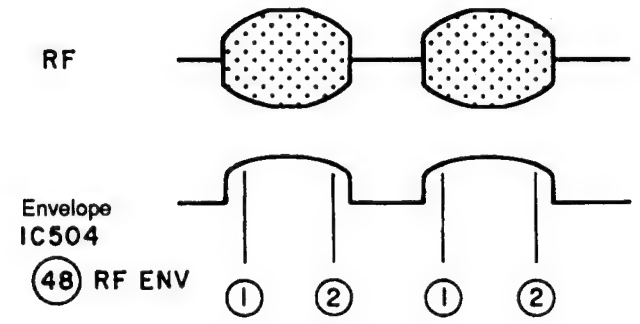


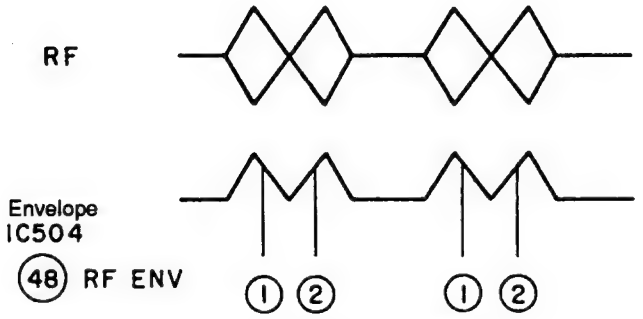
Figure 8-11. Reel Servo Target Speed Values

8.6.2 RF Envelope Servo

This servo is provided for the necessary portion in the PCM area of the RF waveform to have a large amplitude during variable-speed reproduction (CUE/REVIEW). Since the RF waveform is not generated in full amplitude during variable- speed reproduction, the resulting sound may contain much noise if reproduced as is. To solve this problem, the shape (tracking) of the RF waveform is controlled so that a certain portion in the PCM area which is most suitable for reproduction has the largest level. Actually, this is done by reducing the level difference between two points (1) and (2) on the RF envelope to zero as shown in Figure 8-12. Whether the RF waveform becomes a concave or convex depends on which side of (1) or (2) is subtracted from which side. By considering the track-crossing shape, it has been observed that better reproduction (few errors) is obtained when convex for CUE and when concave for REVIEW. Also note that the positions (1) and (2) vary depending on LP and SP.



(a) Reproduction in CUE



(b) Reproduction in REVIEW

Figure 8-12. Envelope Servo

9. Mechanical Section

9.1 Name of Each Part (Main Components)

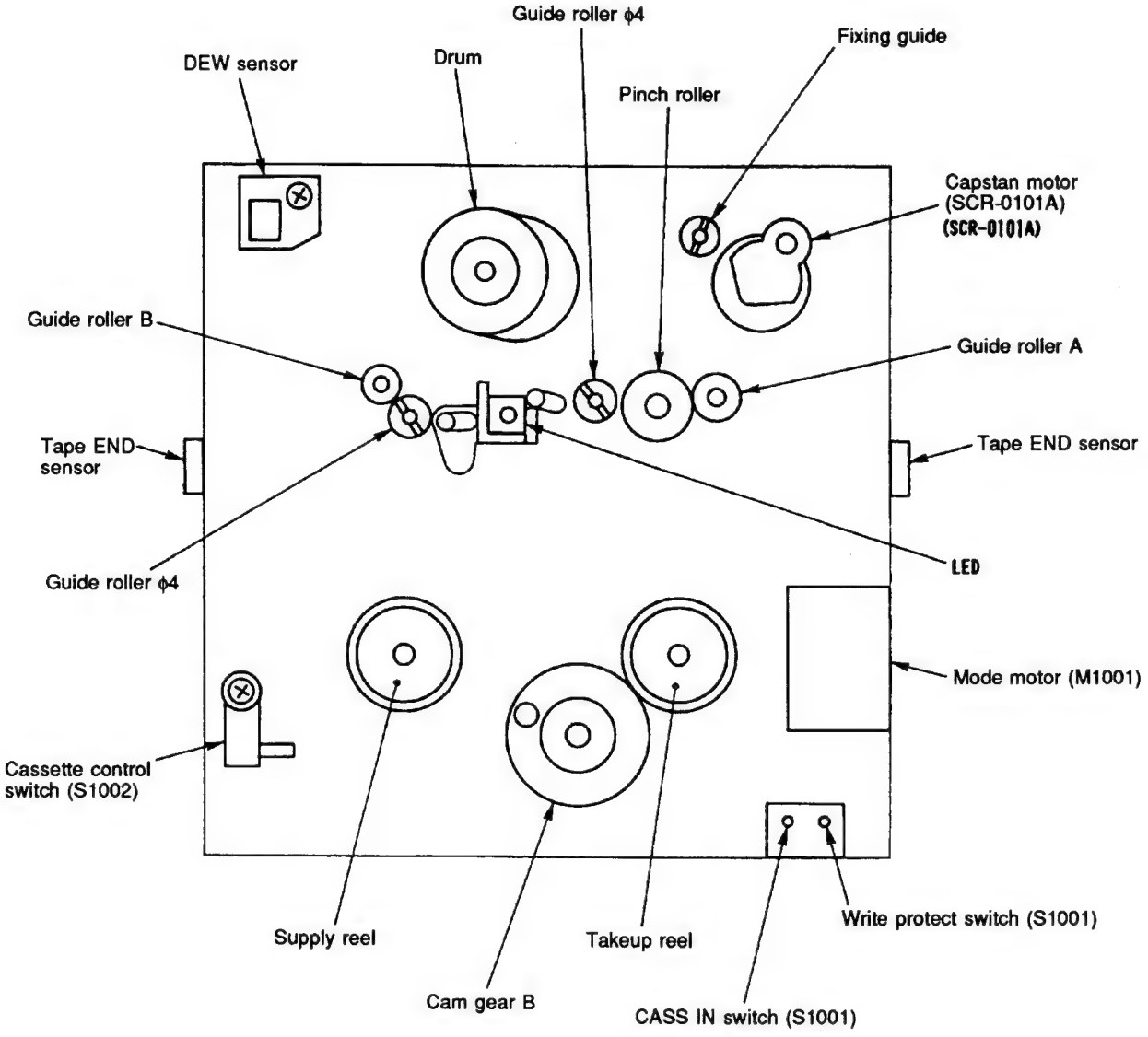


Figure 9-1. Arrangement of Main Components (Top View)

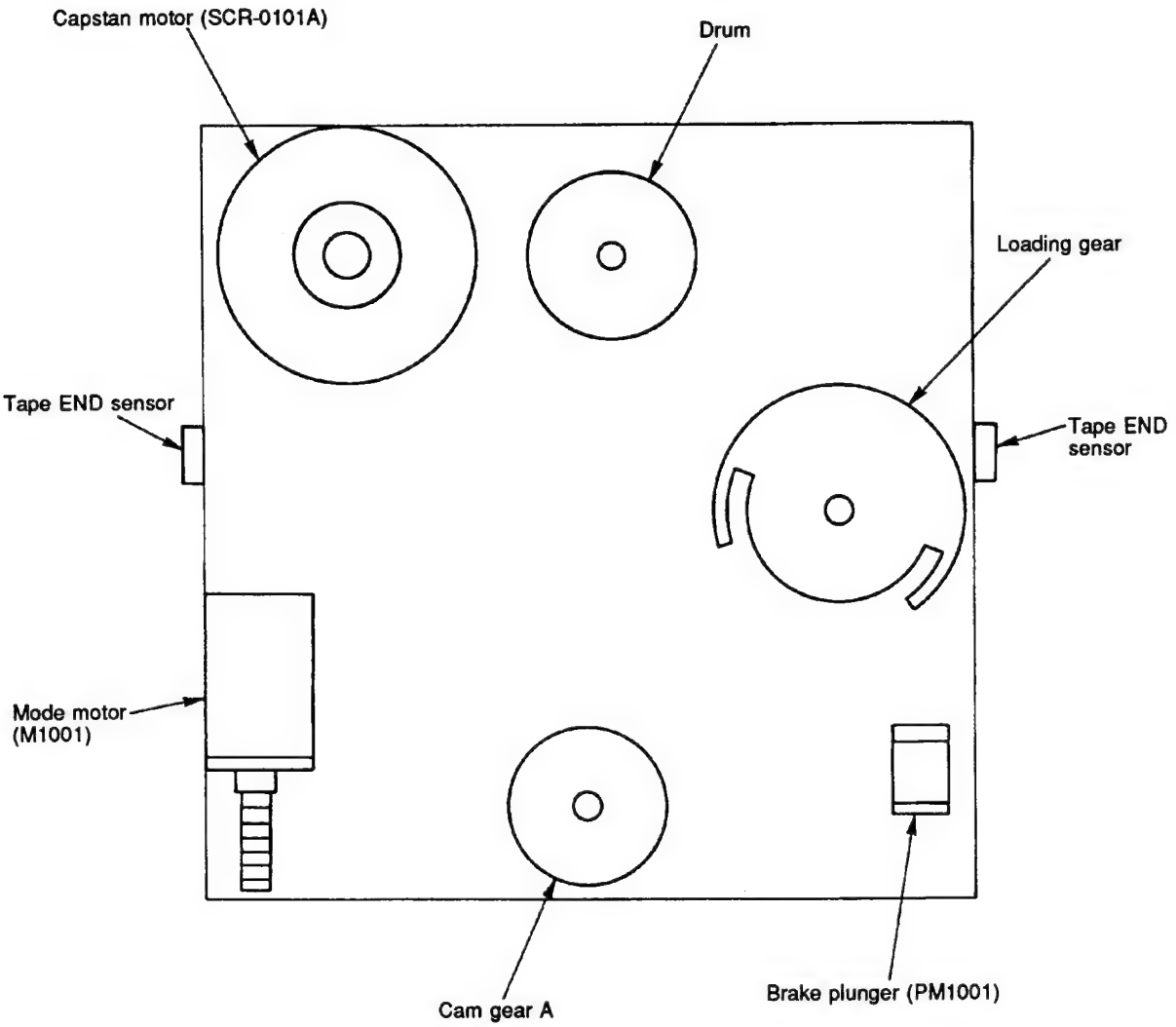


Figure 9-2. Arrangement of Main Components (Reverse Side)

9.2 Cassette IN

9.2.1 Lid OPEN

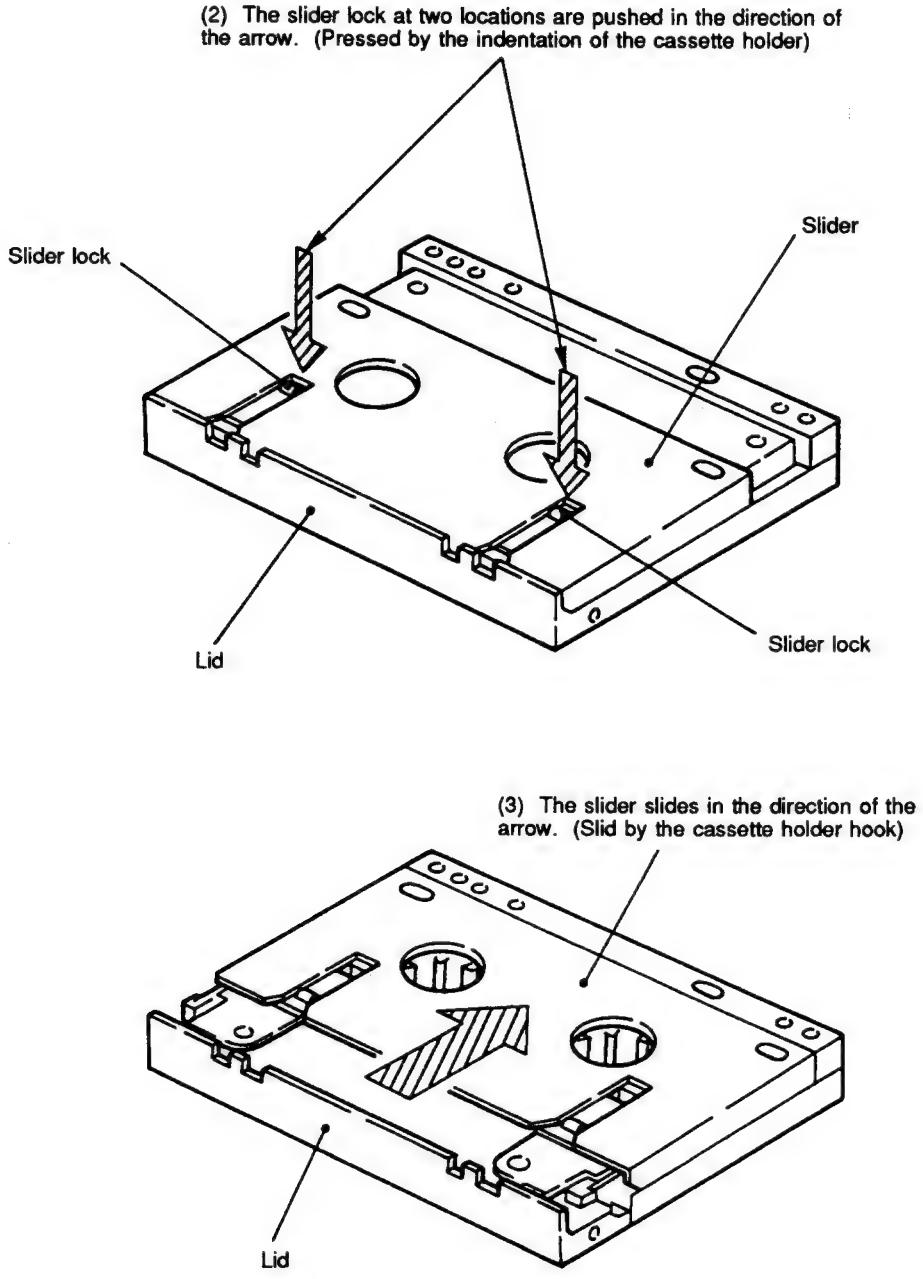


Figure 9-3. Cassette

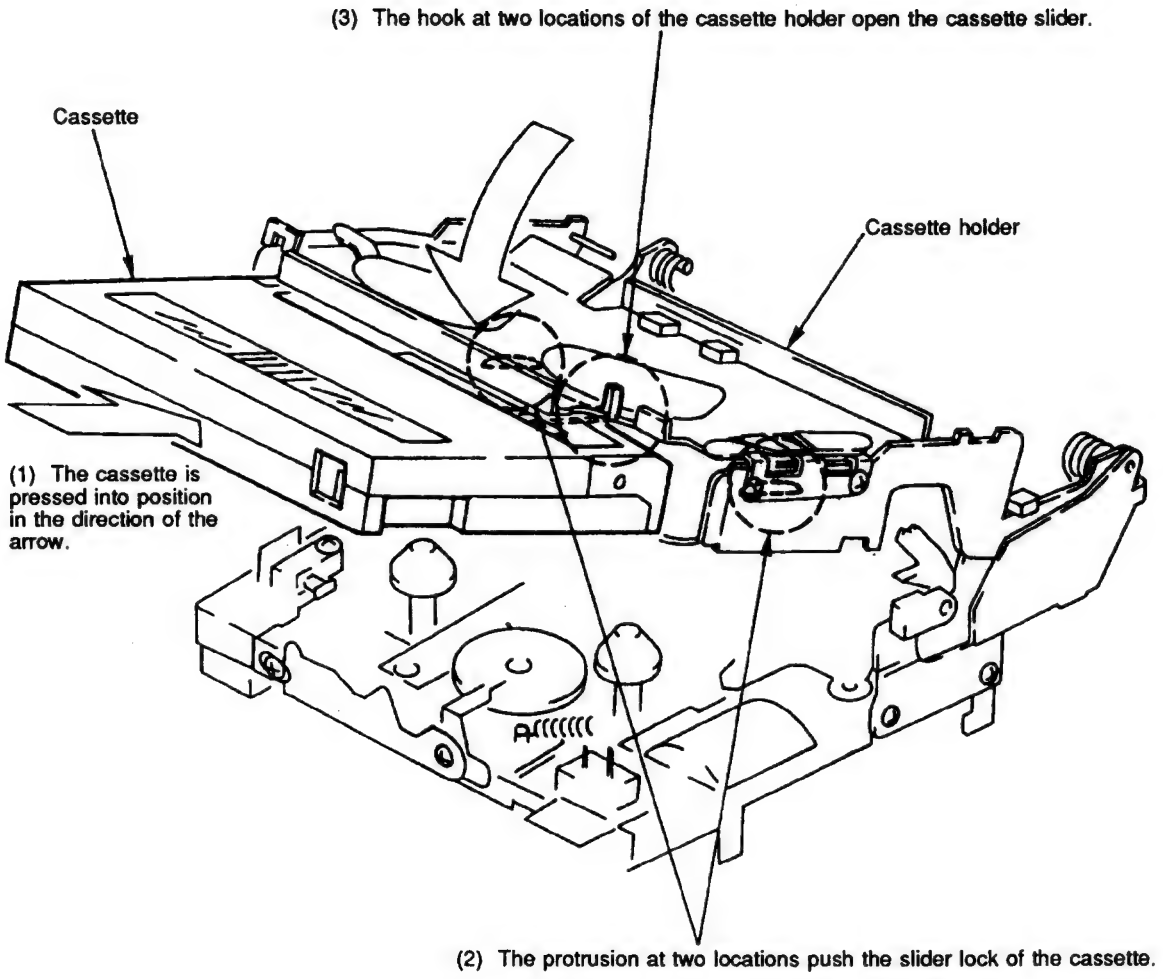


Figure 9-4. Cassette IN

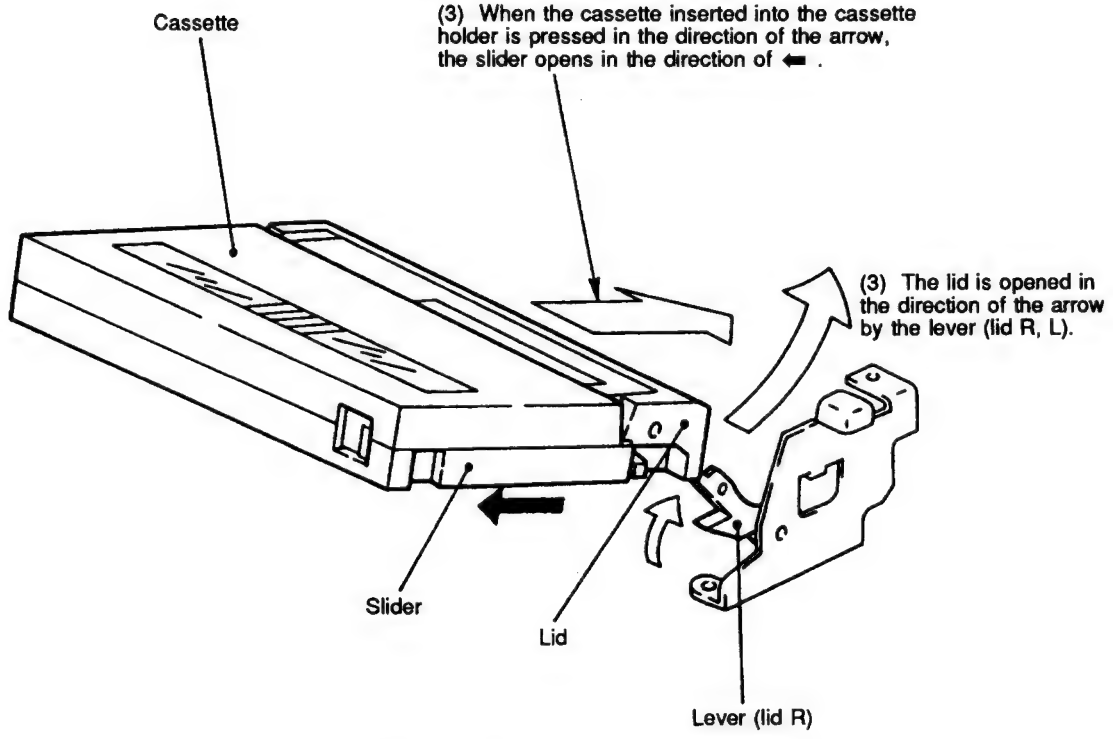


Figure 9-5. Lid OPEN

9.2.2 Cassette Holder Lock

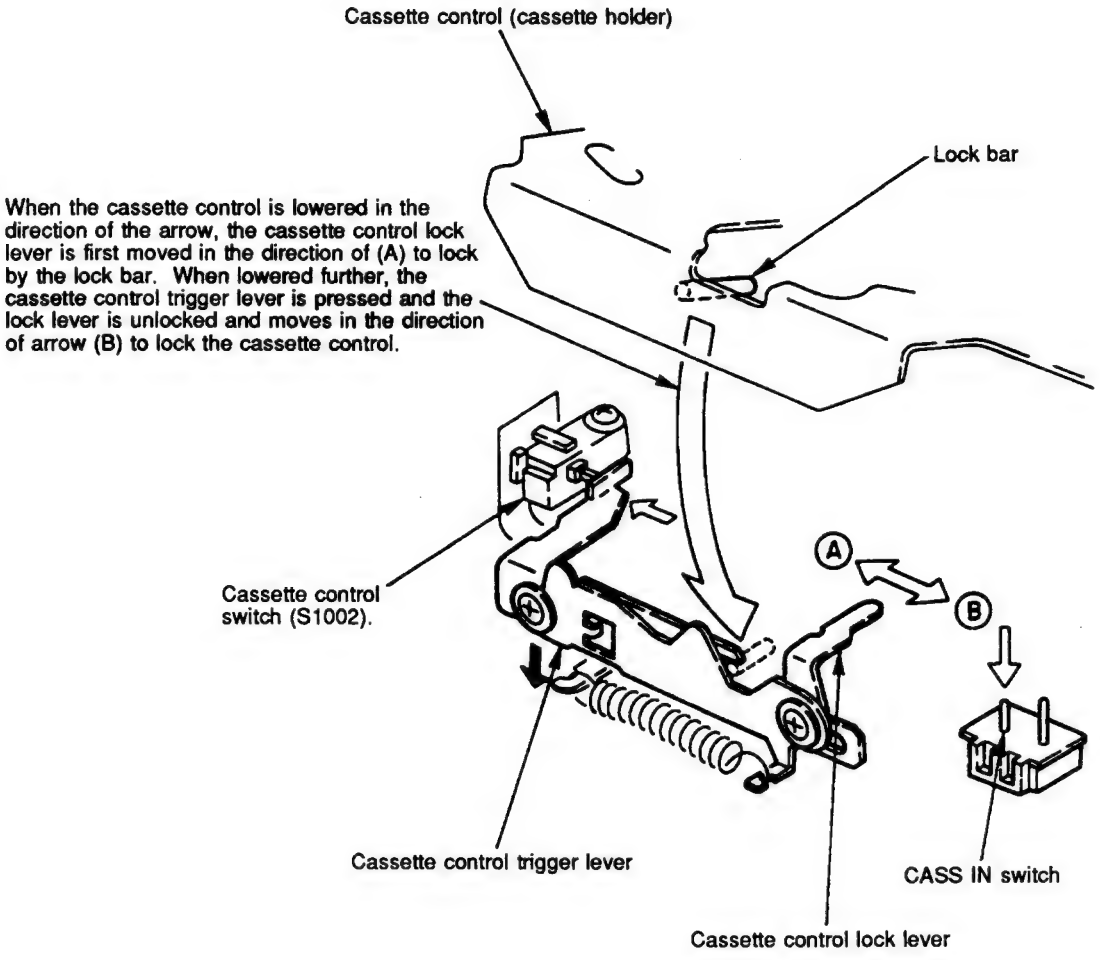
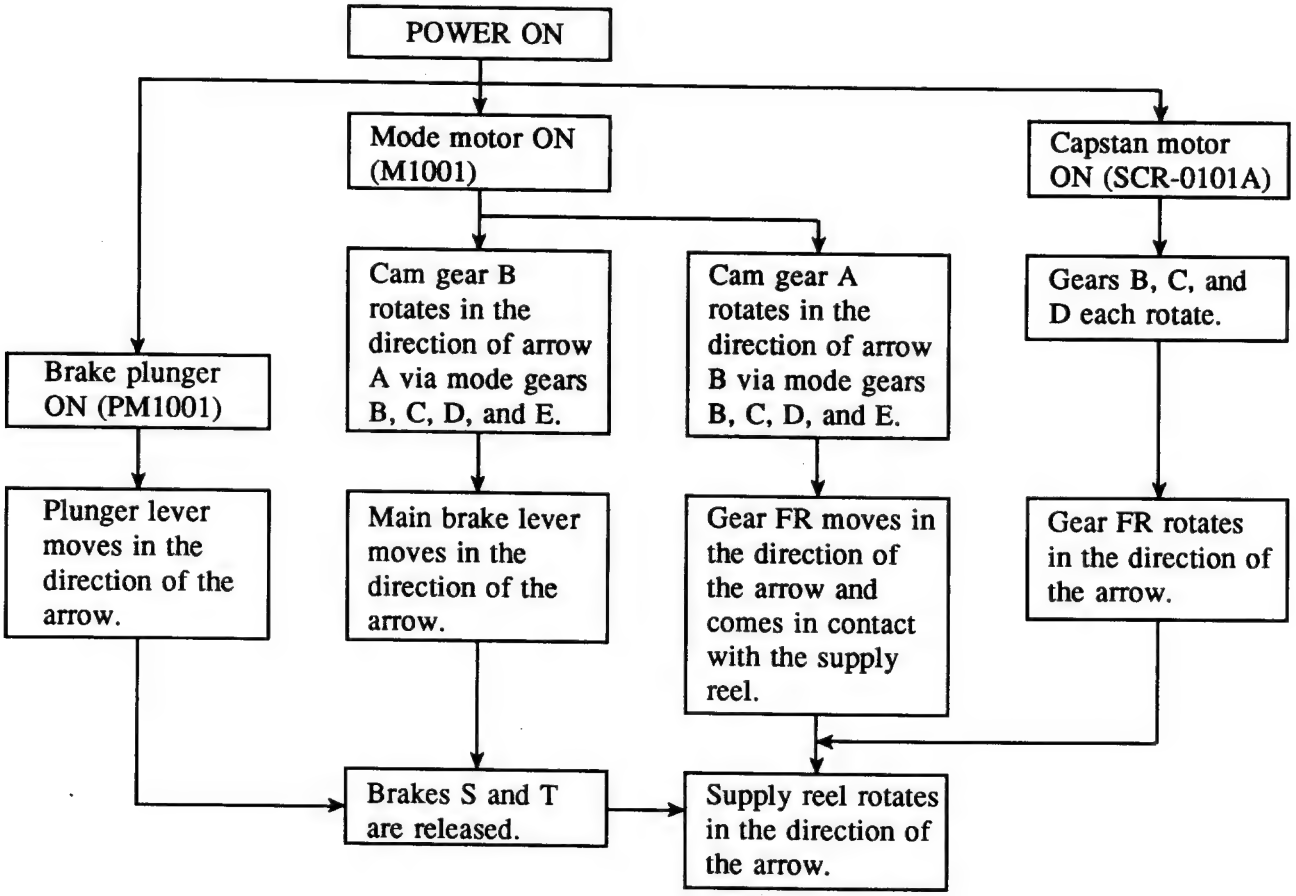


Figure 9-6. Cassette holder lock

9.3 POWER ON



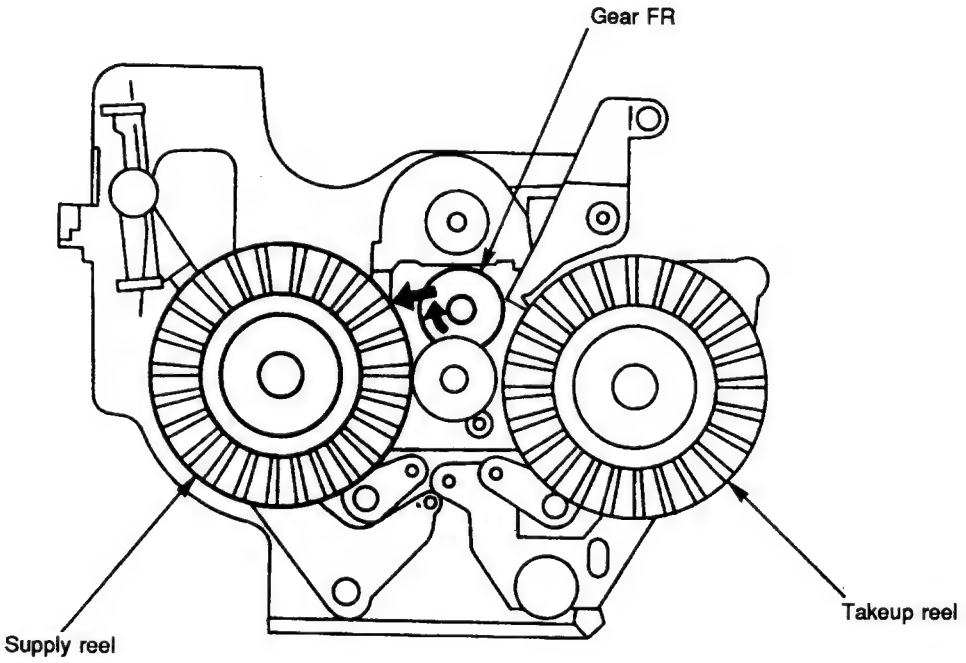


Figure 9-7

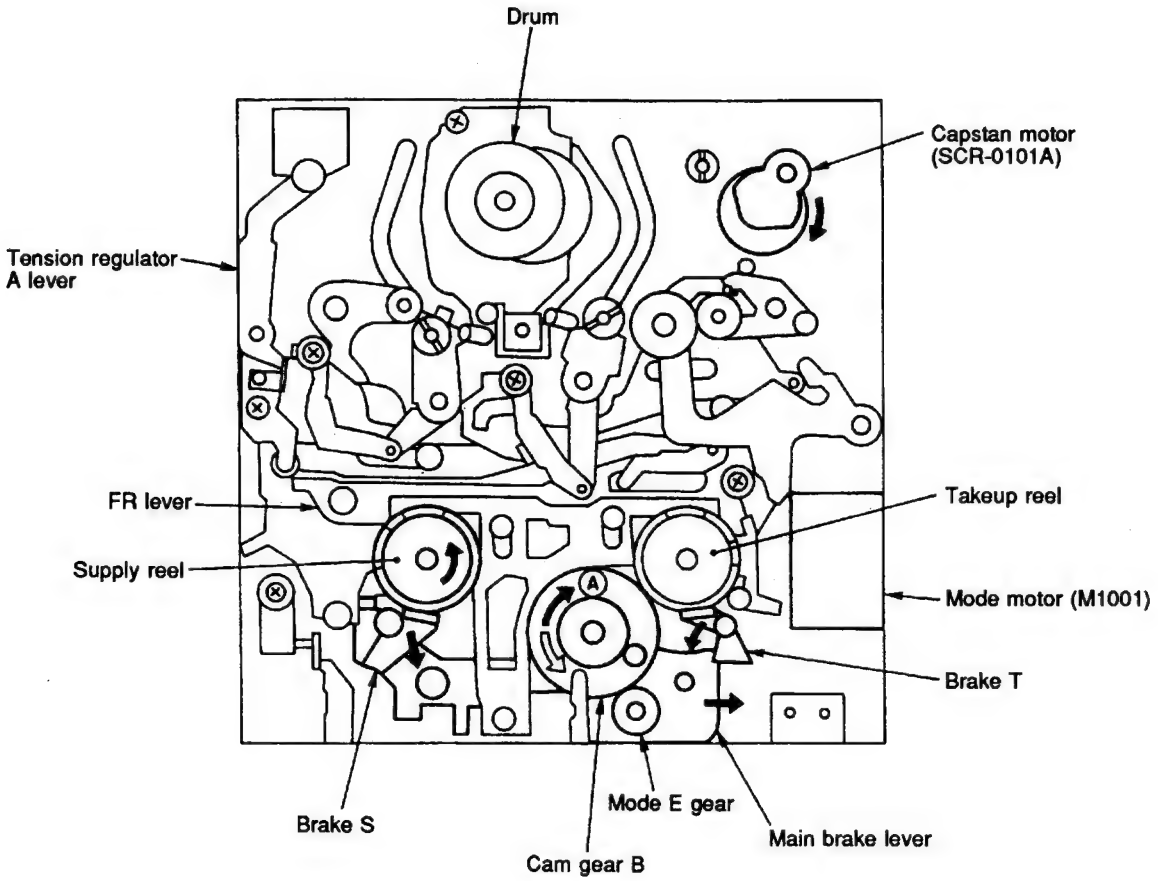


Figure 9-8

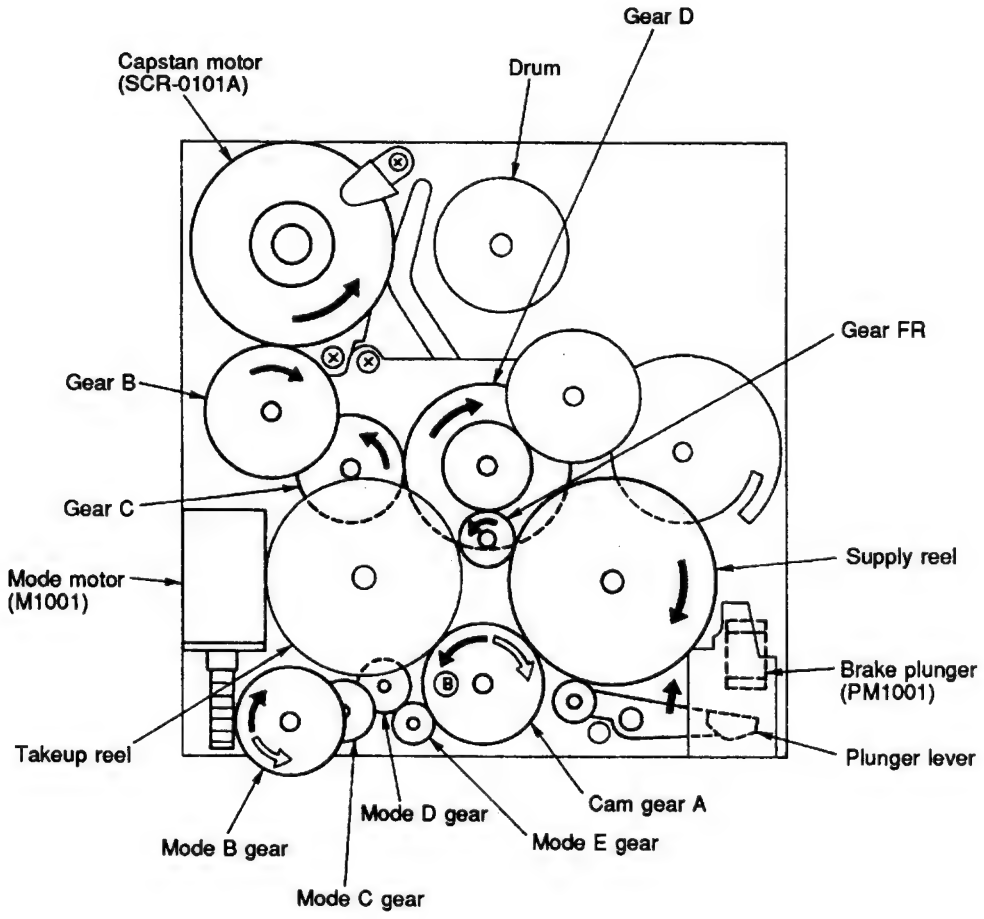
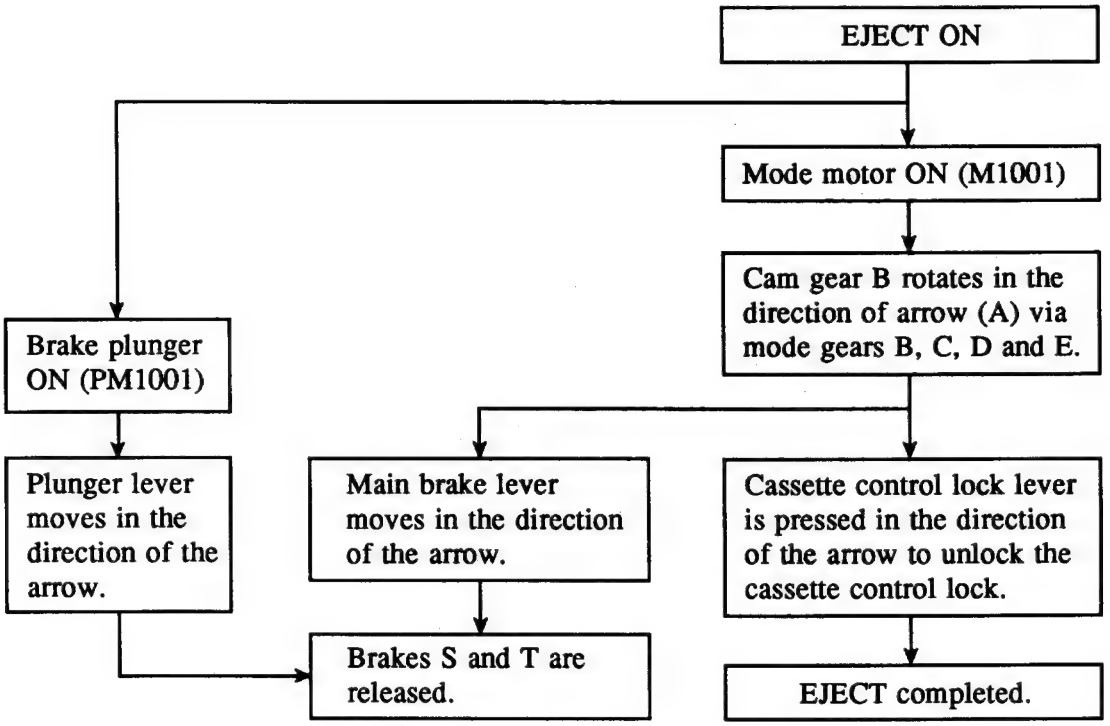


Figure 9-9

9.4 POWER ON → EJECT



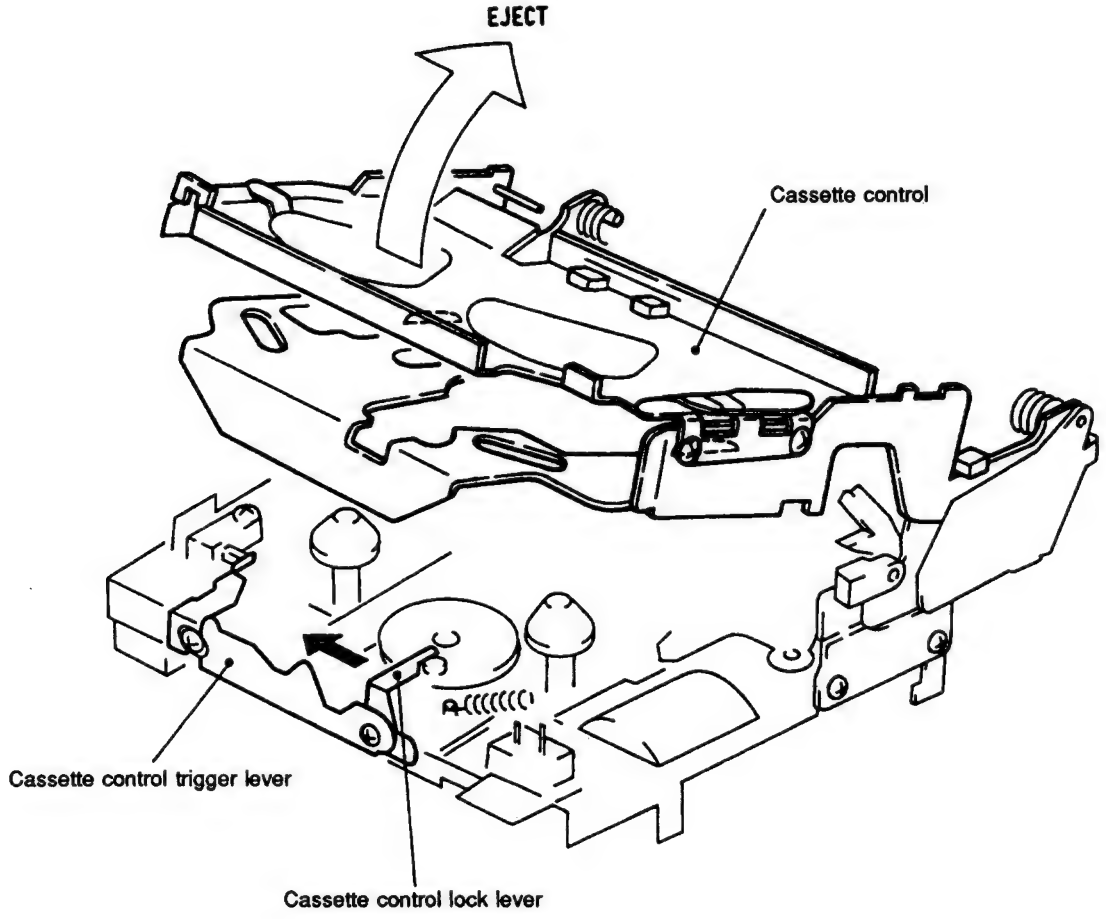


Figure 9-10. EJECT

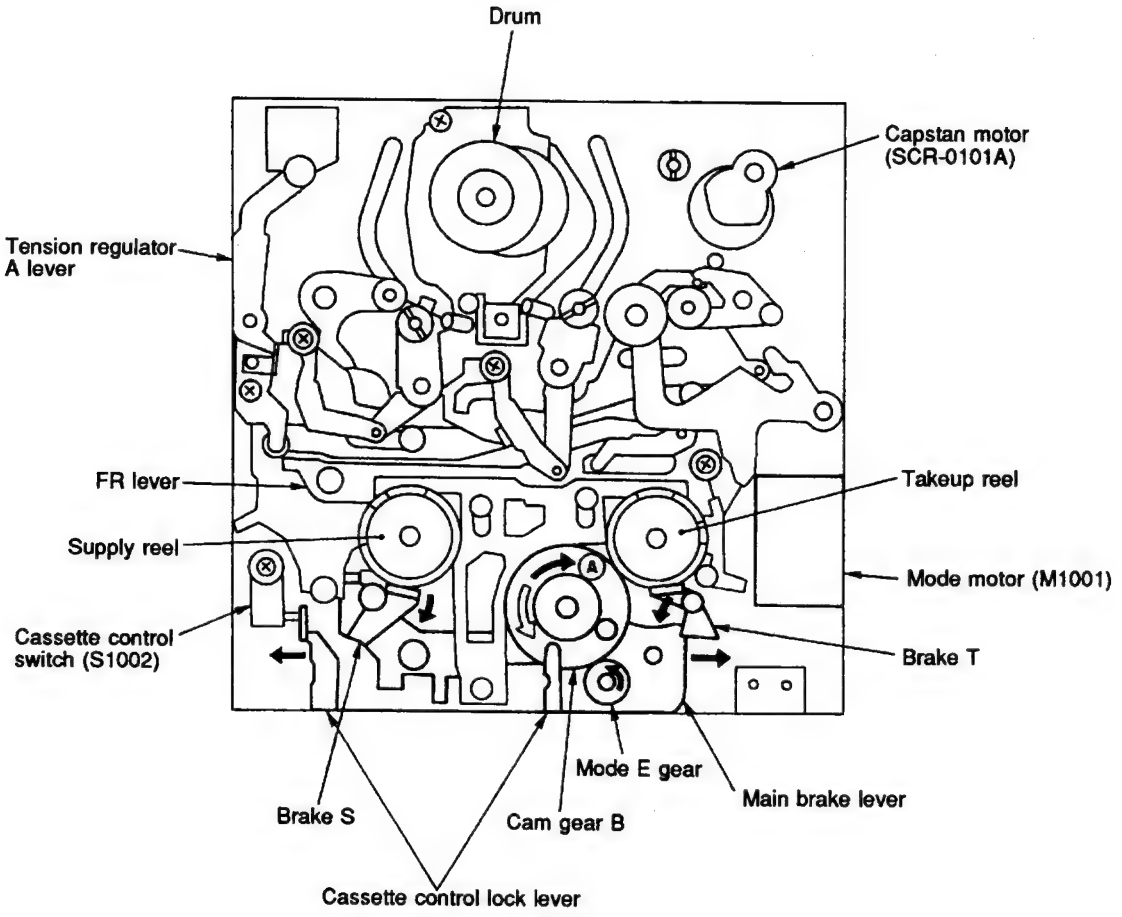


Figure 9-11.

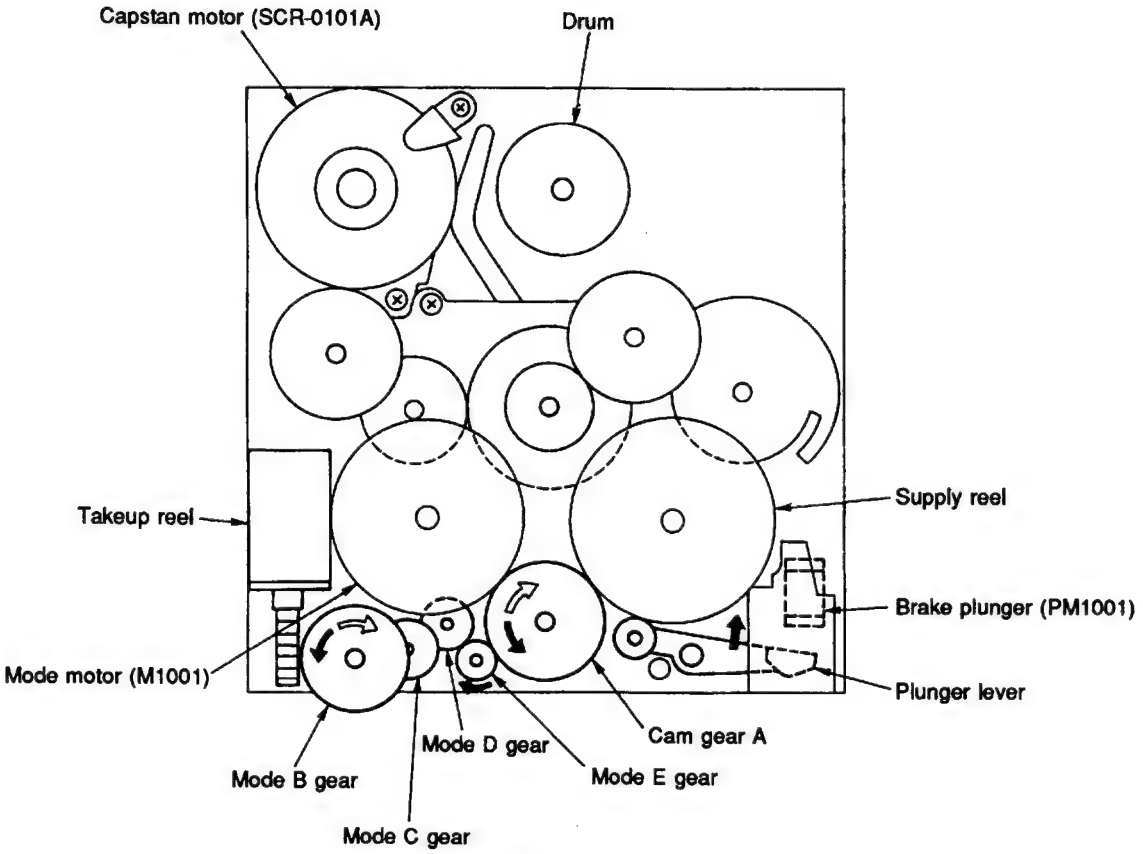


Figure 9-12.

9.5 CASS IN → STOP (Loading)

Cassette control DOWN

Cassette control lever moves in the direction of the arrow to lock the cassette control.

CASS IN switch ON (S1001)

Mode motor ON (M1001)

Capstan motor ON (SCR-0101A)

Cam gear B rotates in the direction of the arrow via mode gears B, C, D, and E.

Cam gear A rotates in the direction of the arrow via mode gears B, C, D, and E.

Loading gear rotates in the direction of the arrow via gears B, C, D, and E.

FR lever moves in the direction of the arrow to release the soft brake, brake RBT, and tension regulator lever brake.

Lever moves in the direction of the arrow to release brakes S

Gear FR moves in the direction of the arrow and comes in contact with the supply reel.

Loading lever moves in the direction of the arrow, and the pinch roller, two guide rollers ϕ4, and guide rollers A and B move in the direction of the arrow.

Tension regulator A lever moves in the direction of the arrow.

Supply reel rotates in the direction of arrow (A).

Pinch roller comes in contact with the capstan motor and rotates in the direction of arrow (A).

Drum rotates.

Supply reel rotates in reverse.

As the capstan motor rotates in reverse, so does the pinch roller.

Drum stops.

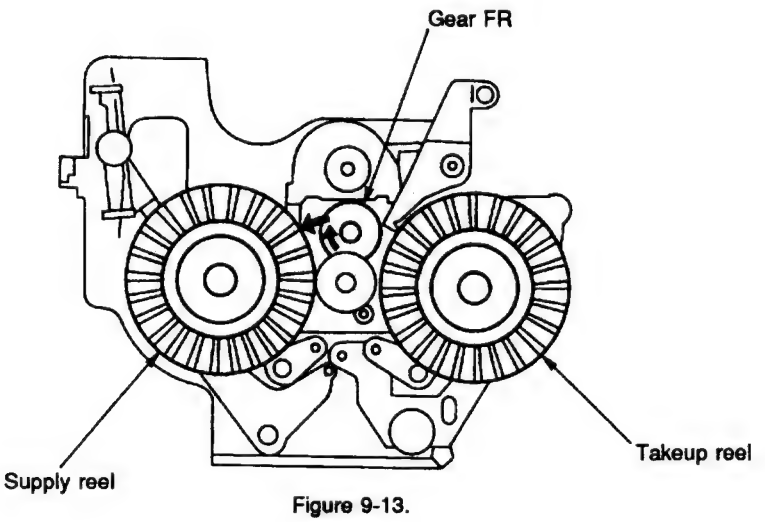
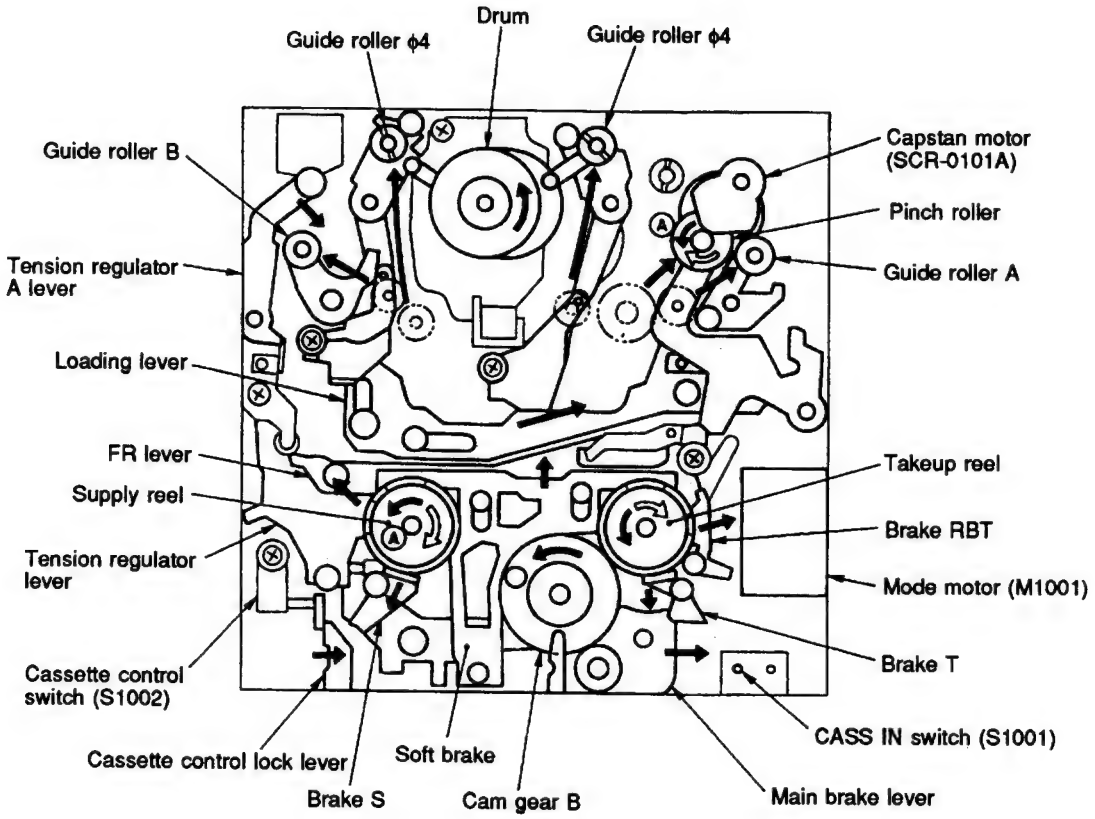


Figure 9-13.



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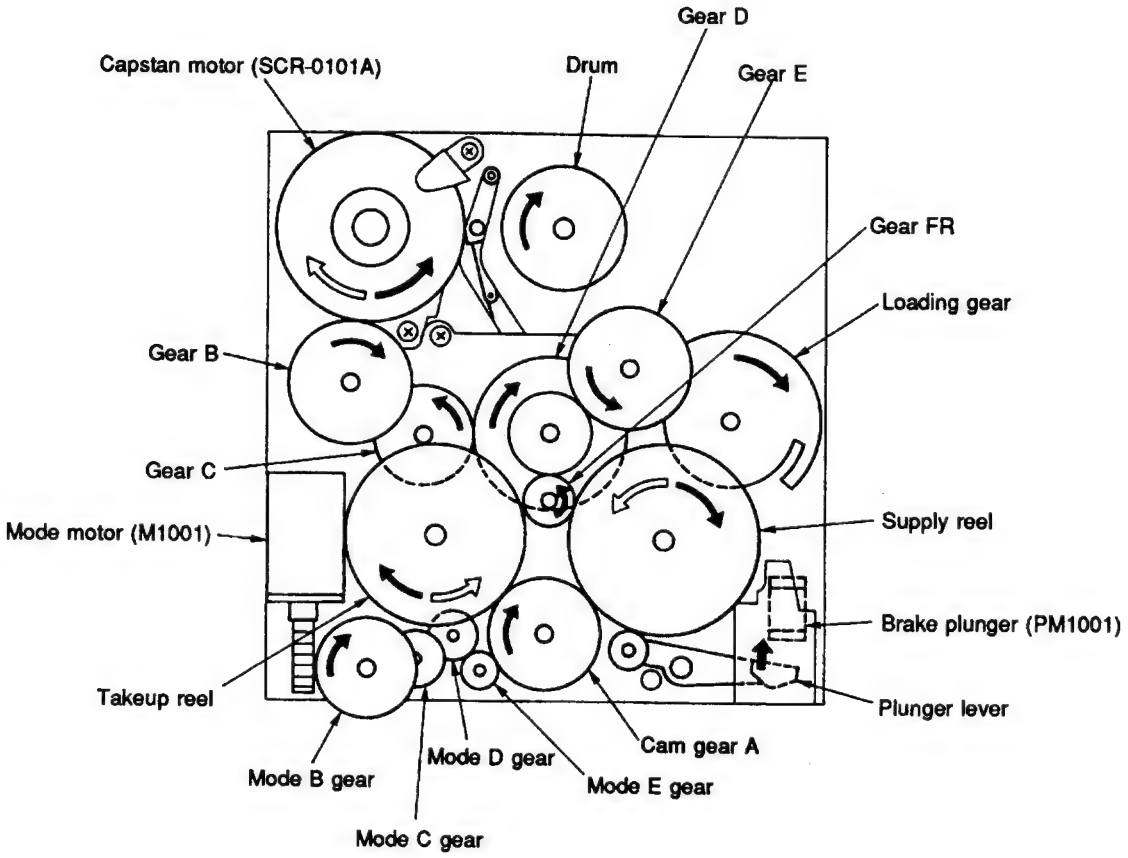
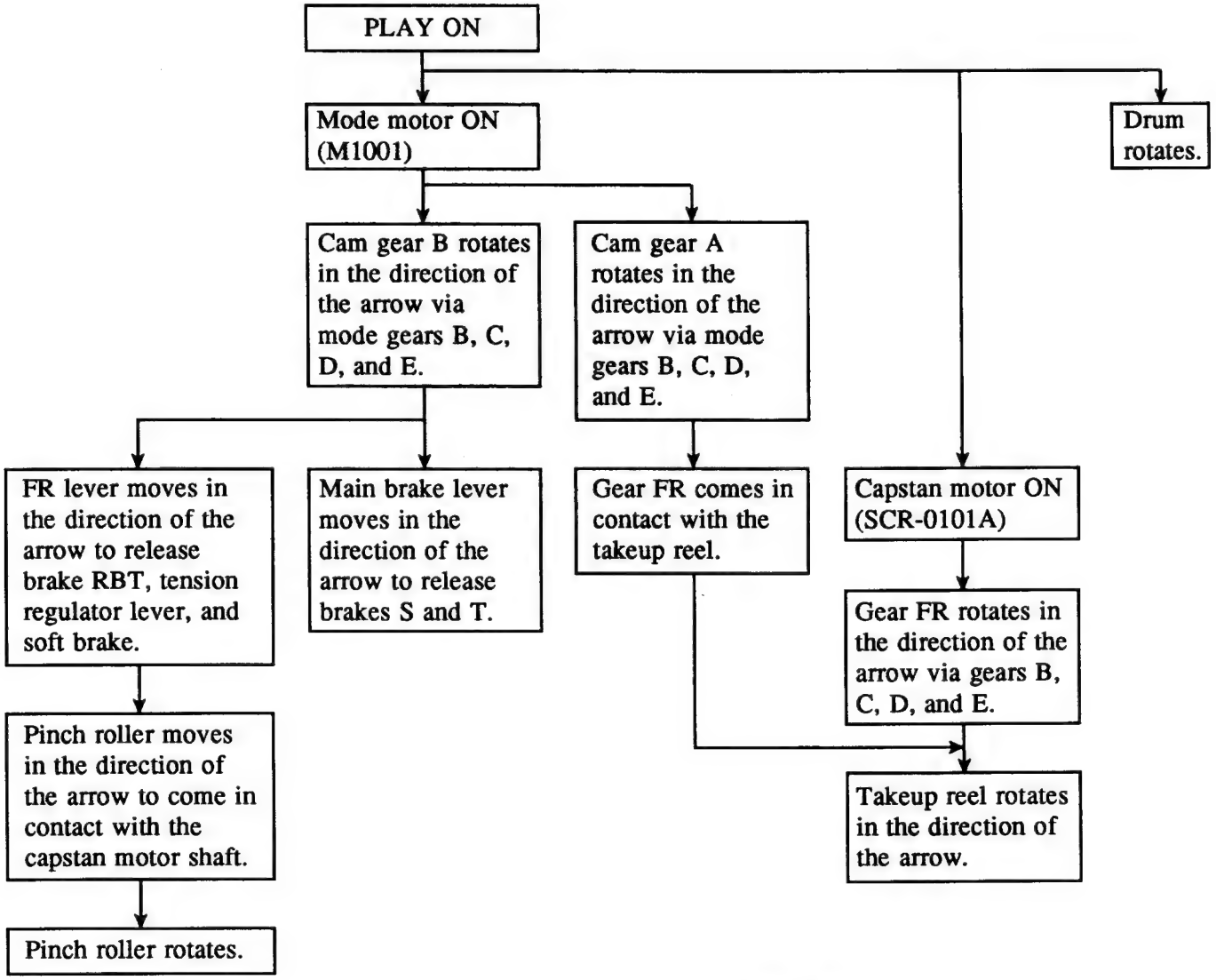
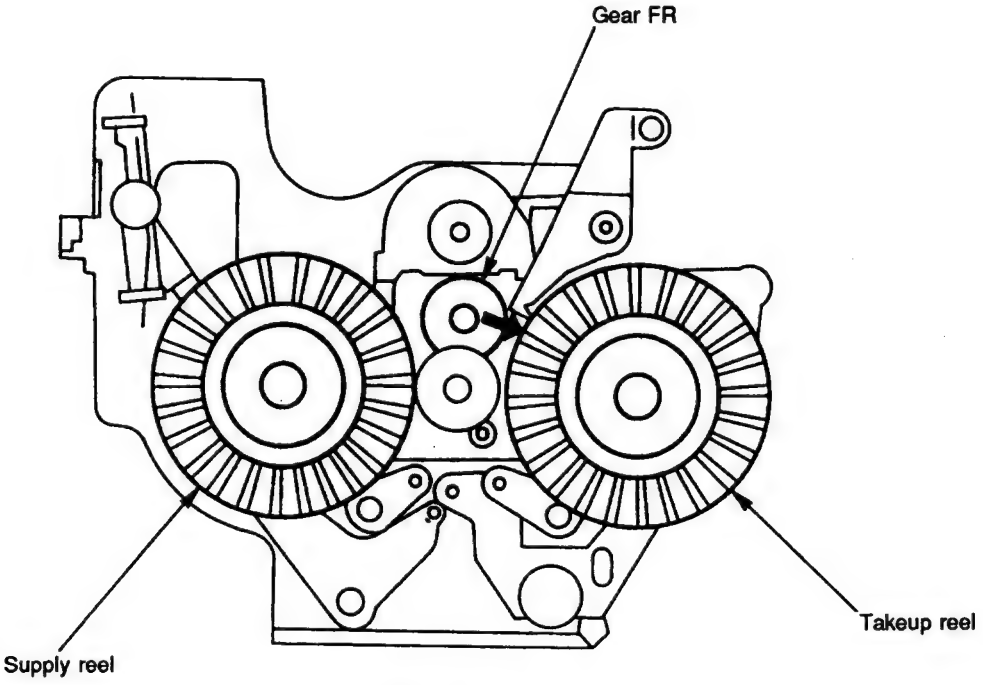


Figure 9-15.

9.6 STOP → PLAY





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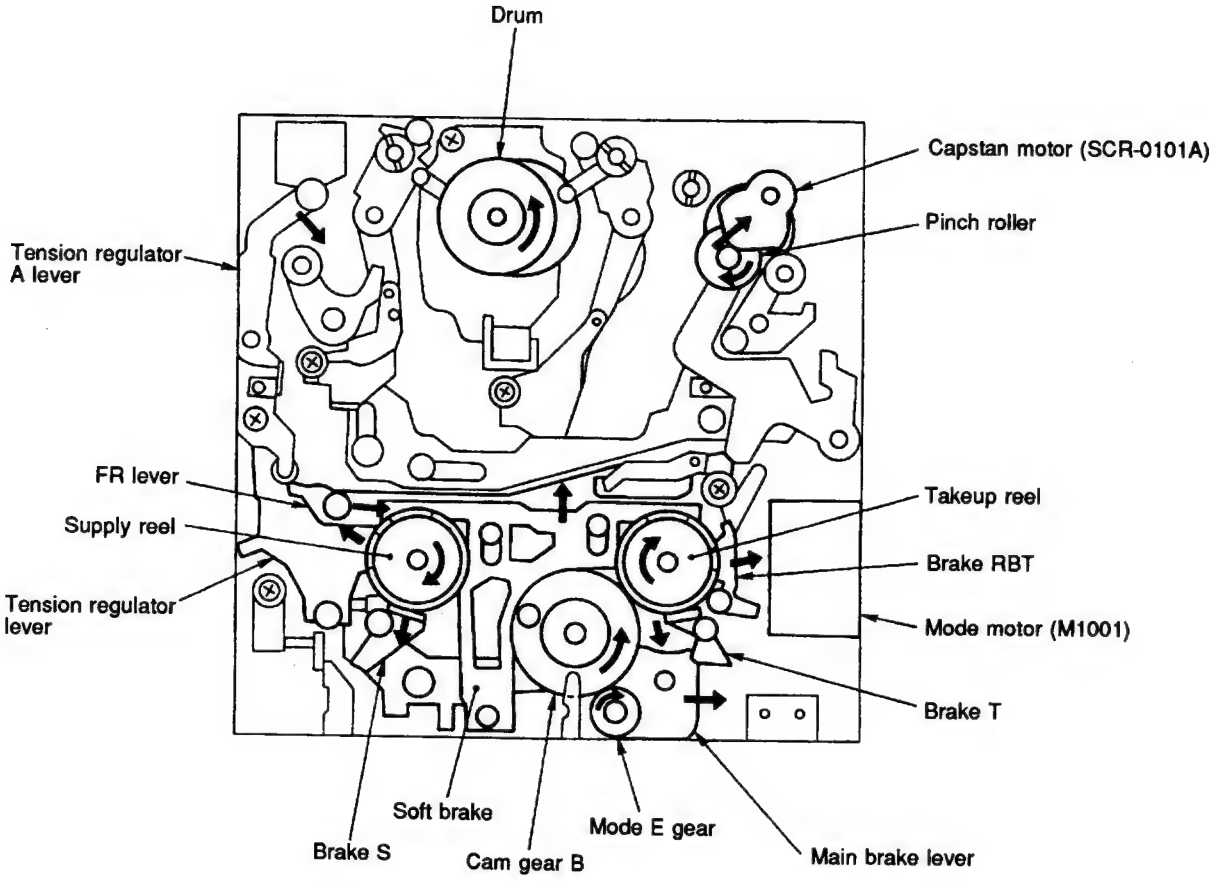


Figure 9-17.

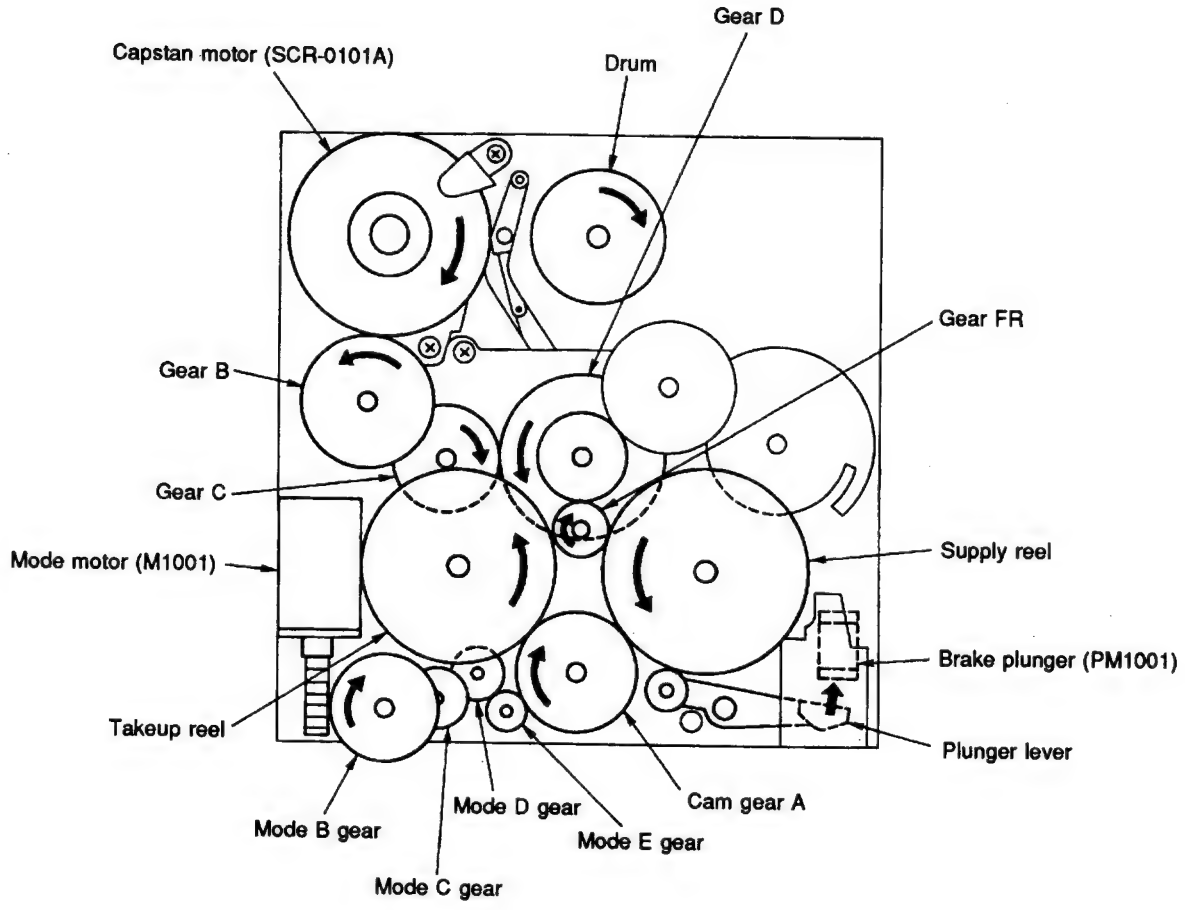
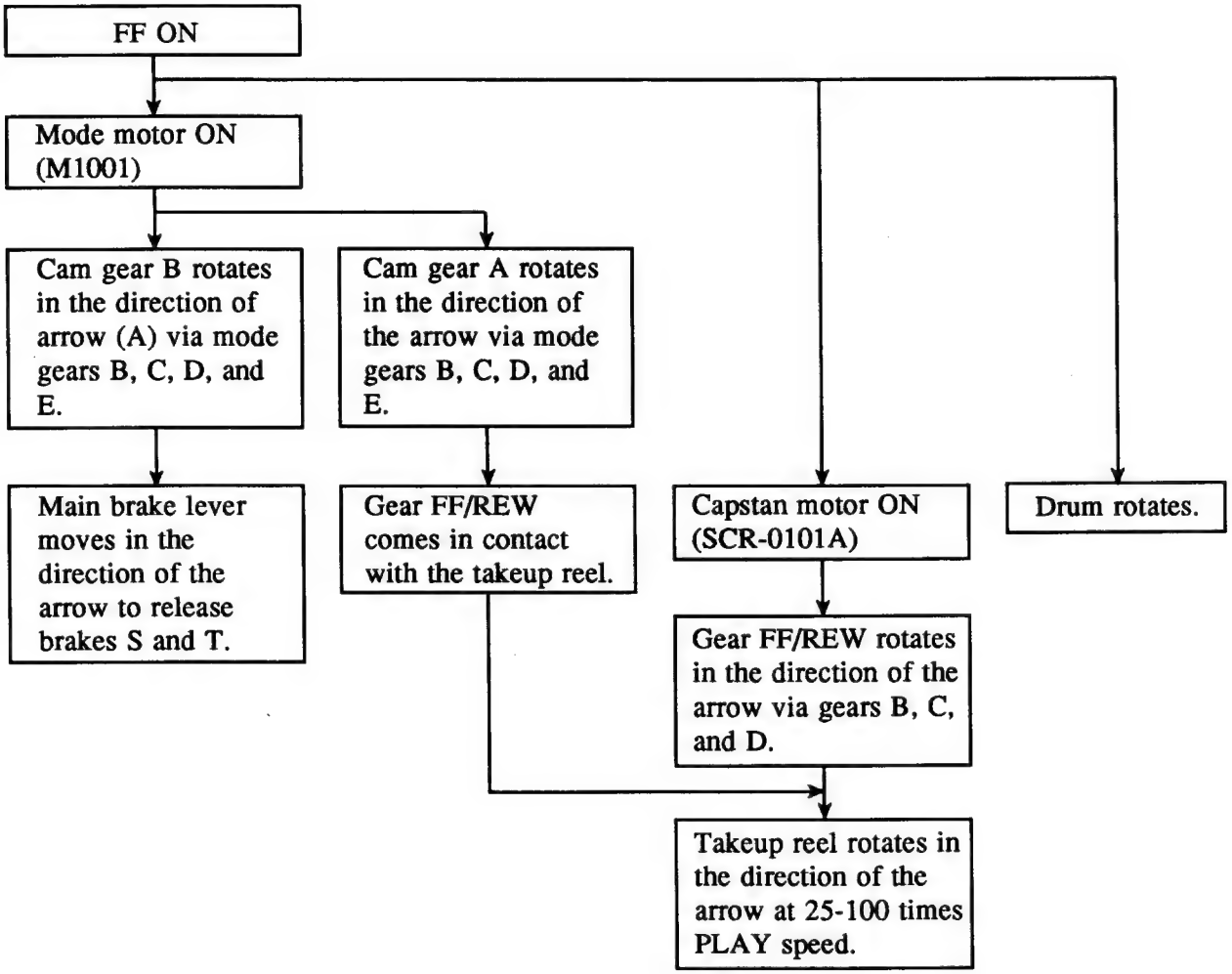
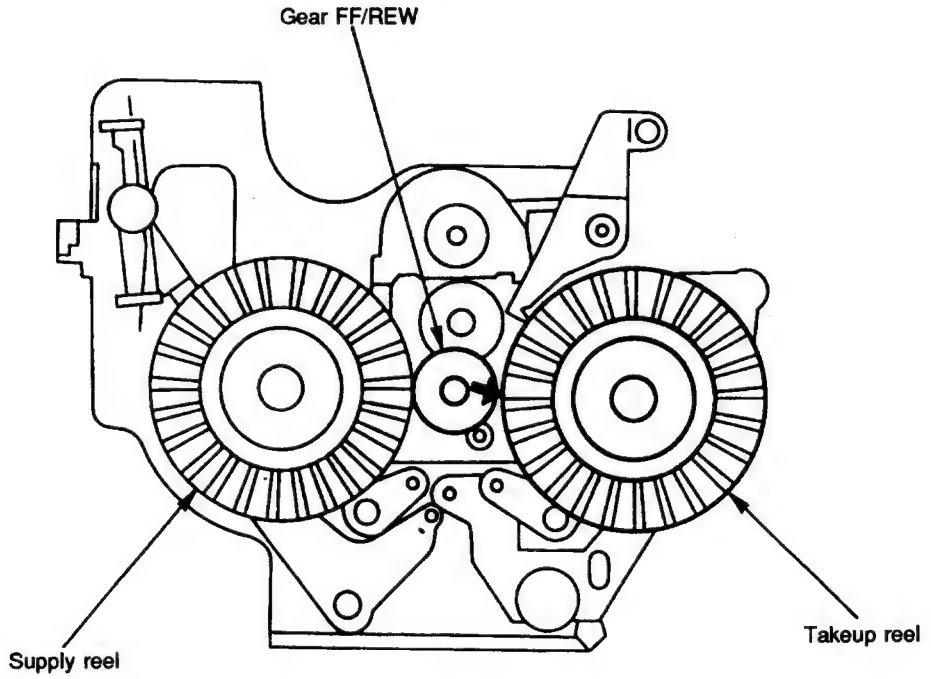


Figure 9-18.

9.7 STOP → FF





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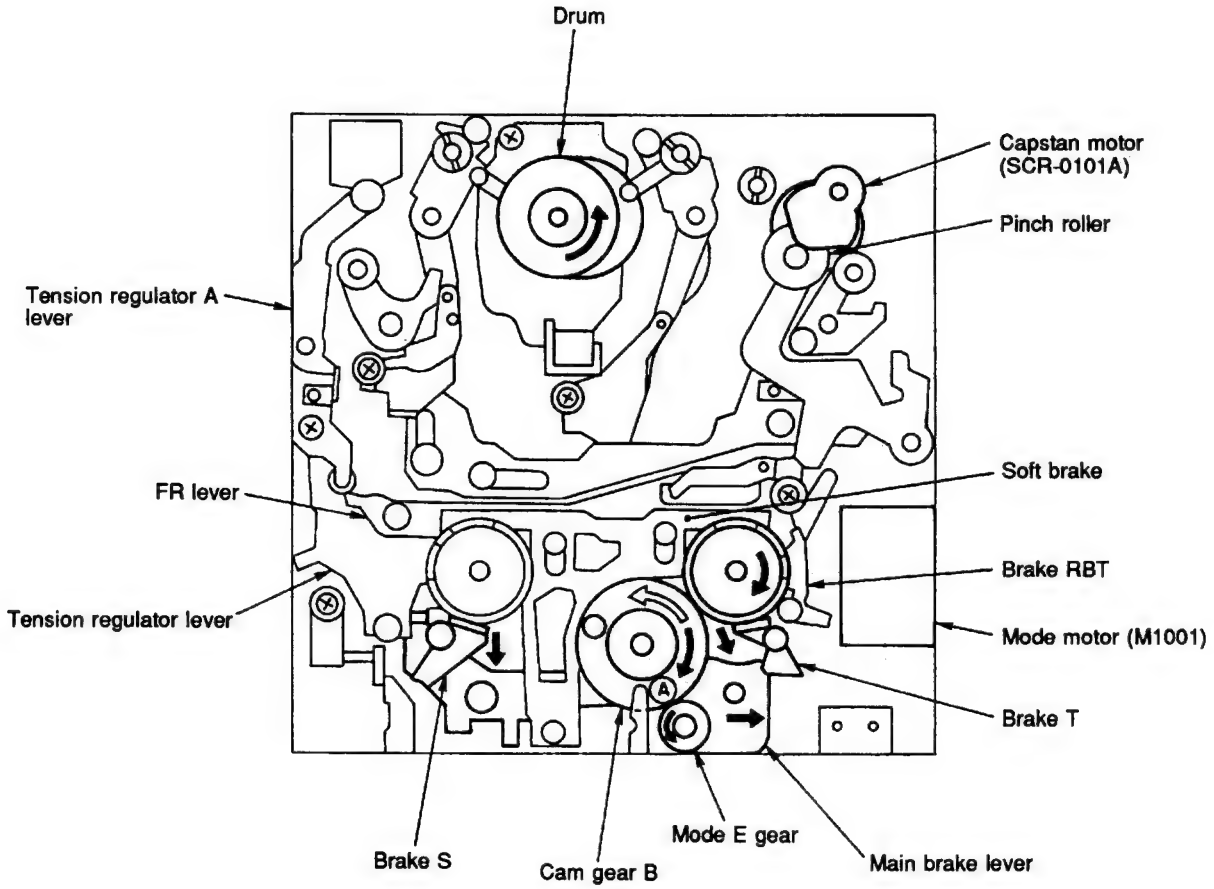

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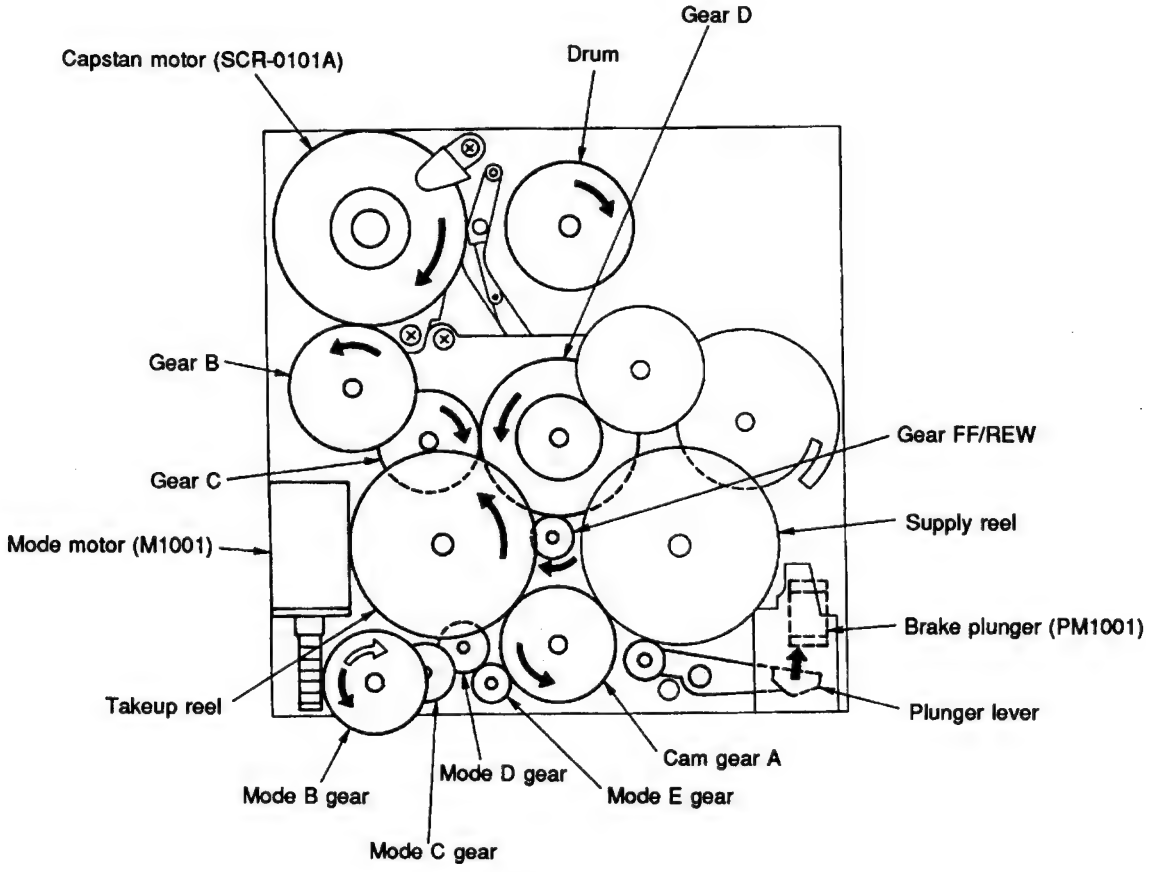
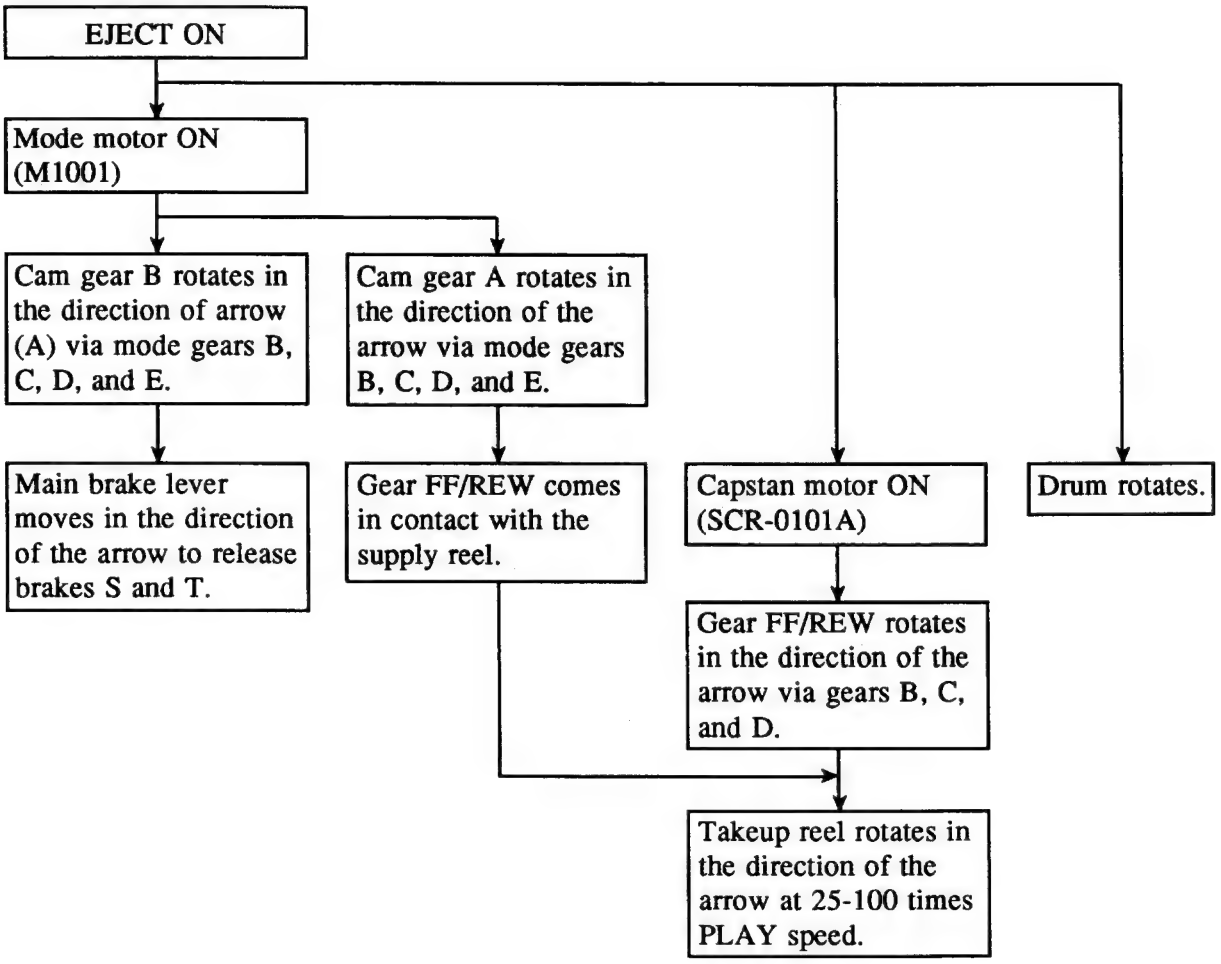


Figure 9-21.

9.8 STOP → REW



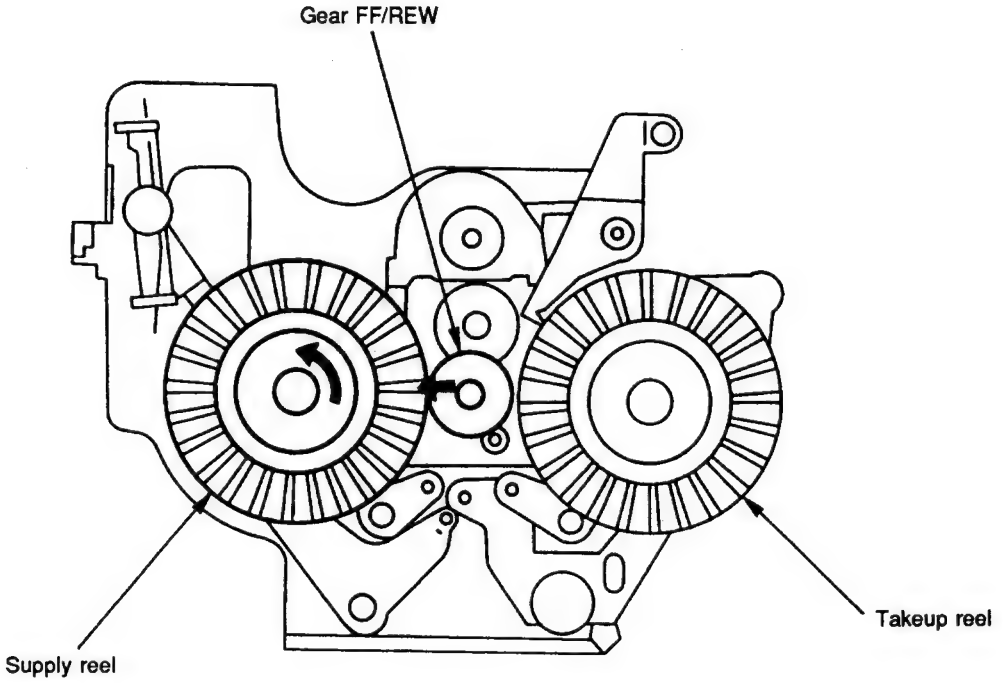
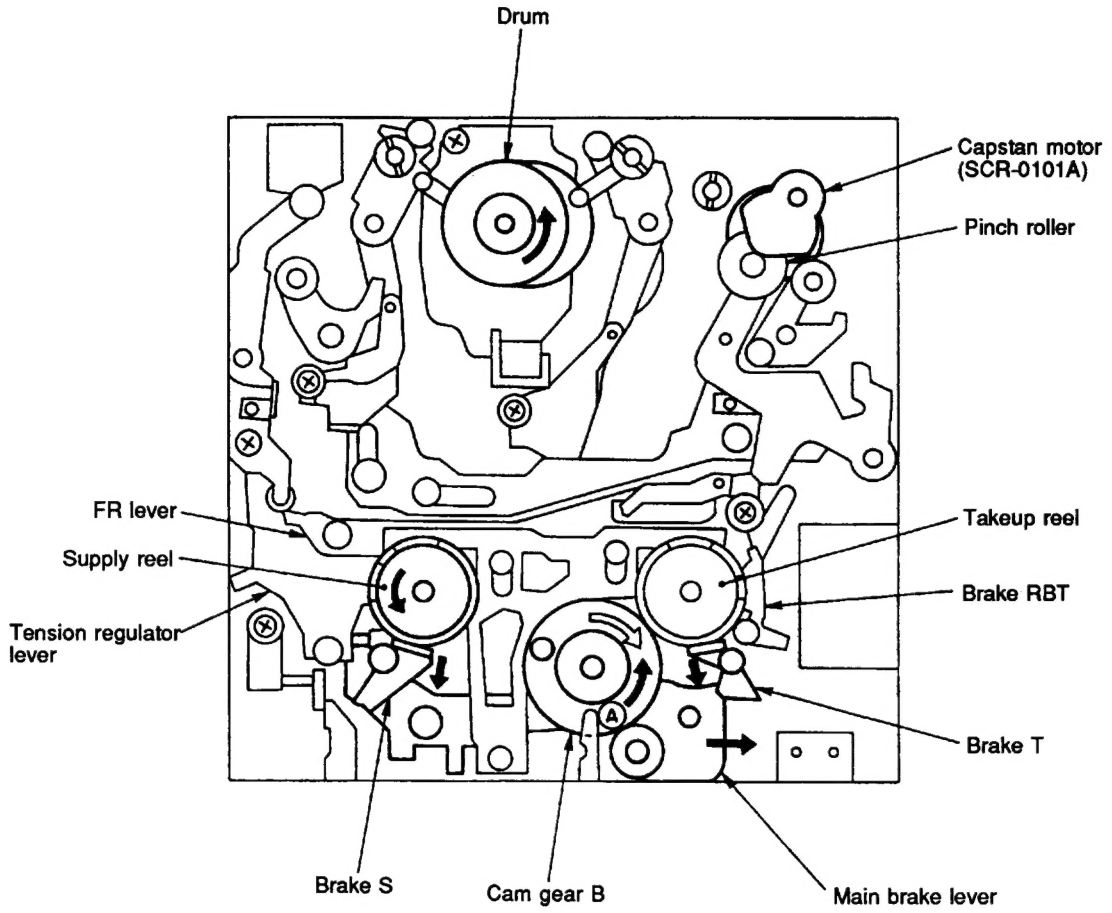


Figure 9-22.



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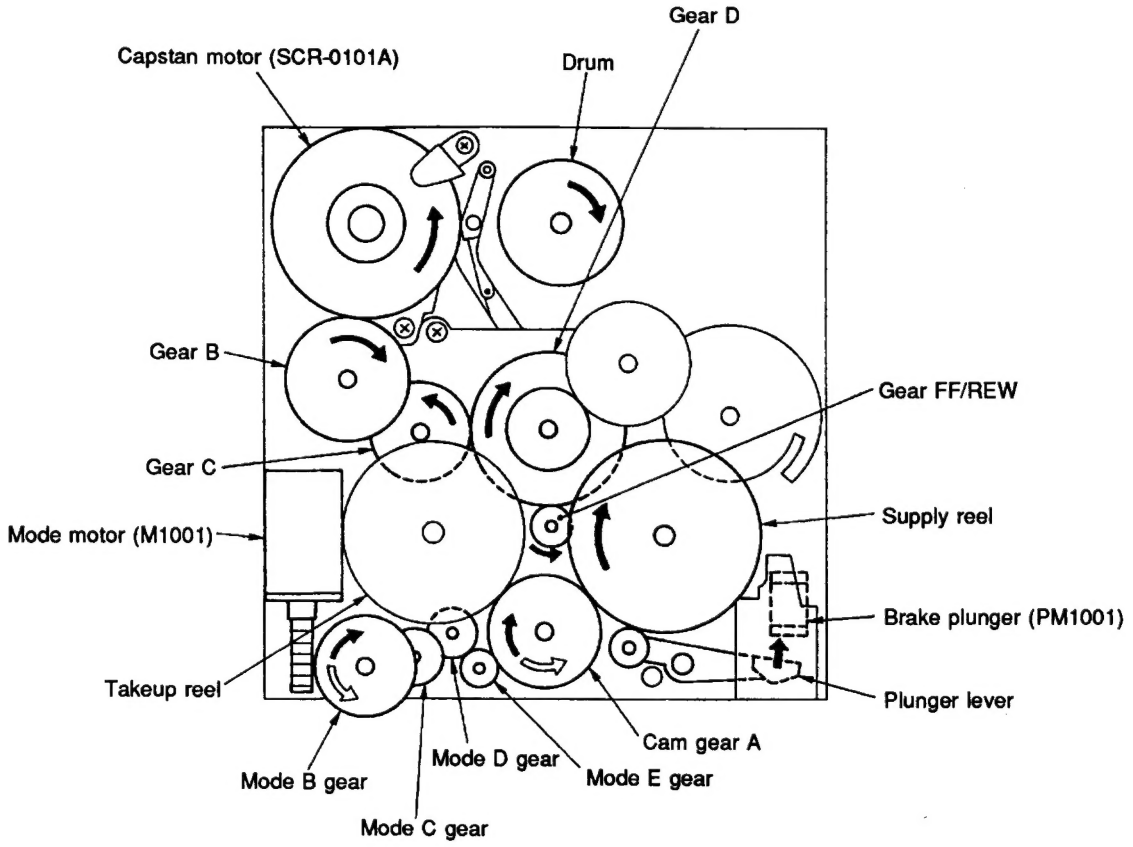

Figure 9-24.

9.9 STOP → EJECT

EJECT ON

Mode motor ON (M1001)

Cam gear B rotates in the direction of arrow (A) via mode gears B, C, D, and E.

Cam gear A rotates in the direction of the arrow via mode gears B, C, D, and E.

FR lever moves in the direction of the arrow to release tension regulator lever, brake RBT, and soft brake.

Main brake lever moves in the direction of the arrow to release brakes S and T.

Gear FR moves in the direction of the arrow and comes in contact with the supply reel.

Capstan motor ON (SCR-0101A)

Tension regulator A lever moves in the direction of arrow (A) to return.

Gear FR rotates in the direction of the arrow via gears B, C, and D.

Loading gear rotates in the direction of the arrow via gears B, C, D, and E.

Supply reel rotates in the direction of the arrow to wind up tape.

Loading lever moves in the direction of the arrow so that two guide rollers ϕ4, guide rollers A and B, and pinch roller move in the direction of the arrow.

Cam gear B further rotates in the direction of arrow (A).

Cassette control lock lever moves in the direction of the arrow to release cassette control lock.

EJECT completed.

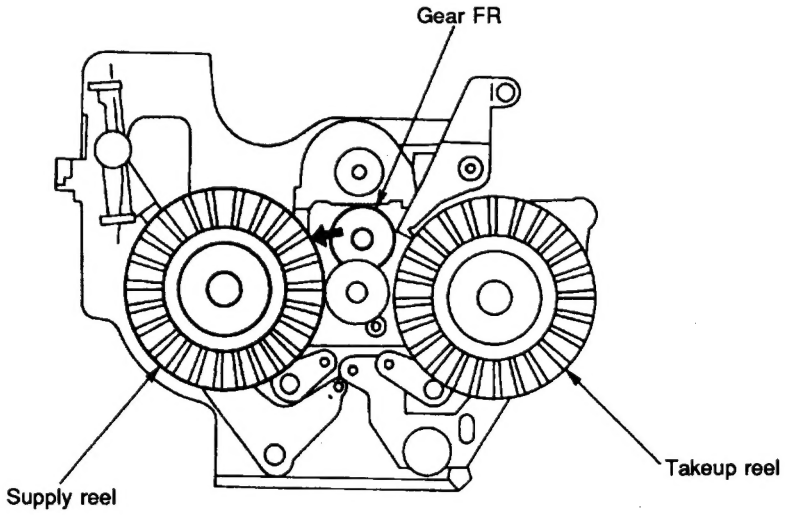

Figure 9-25.

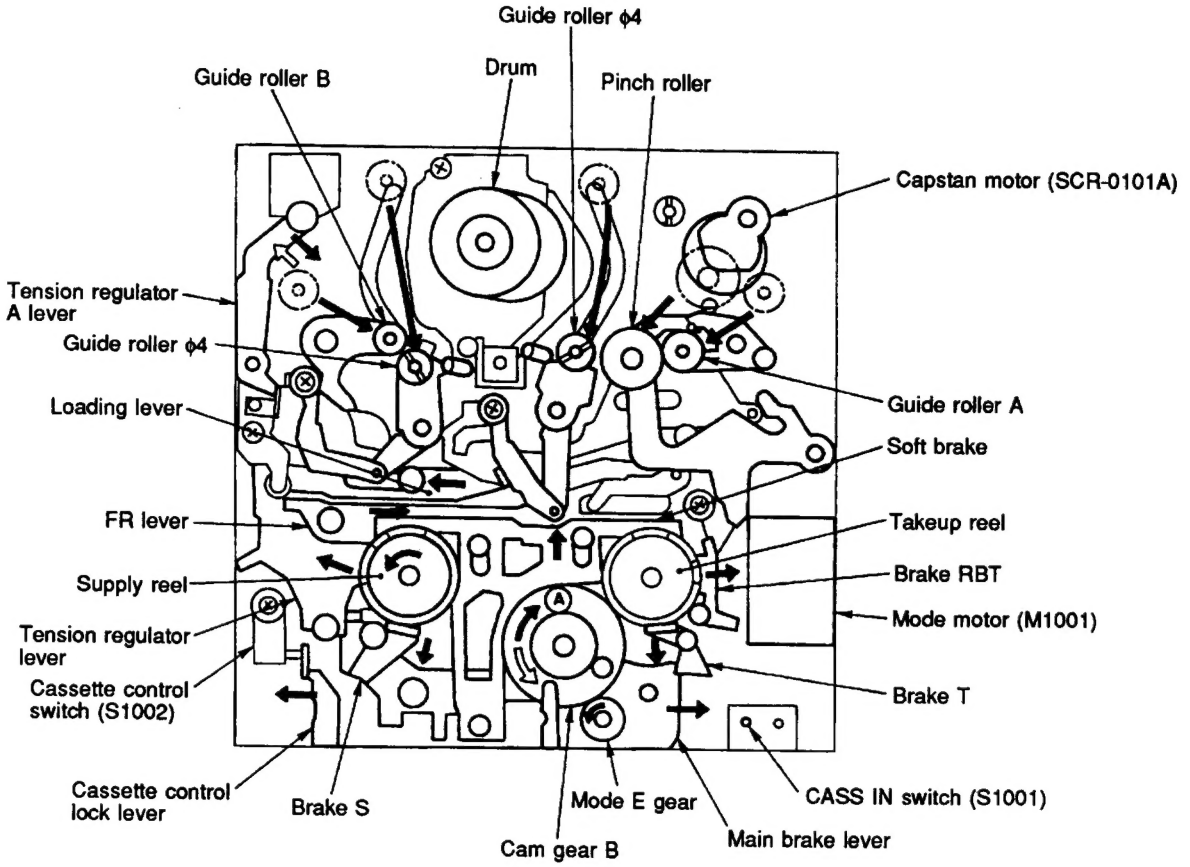

Figure 9-26.

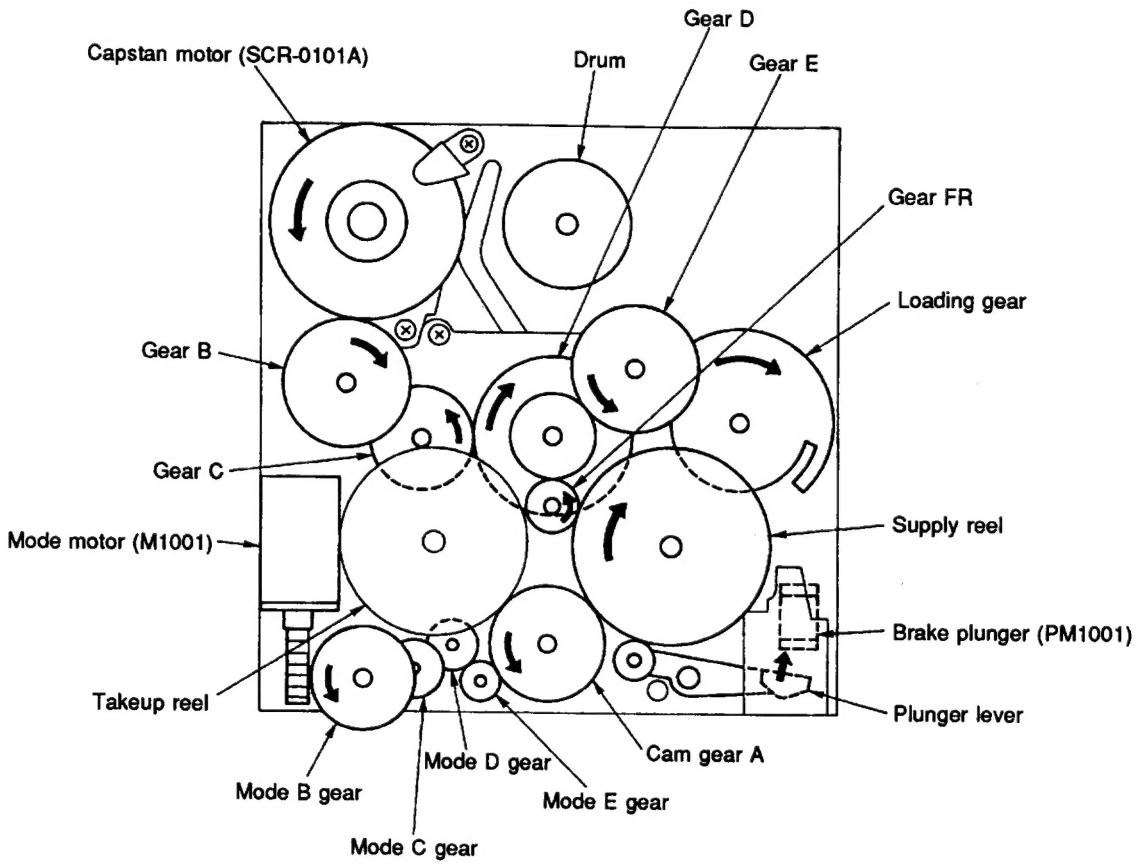

Figure 9-27.

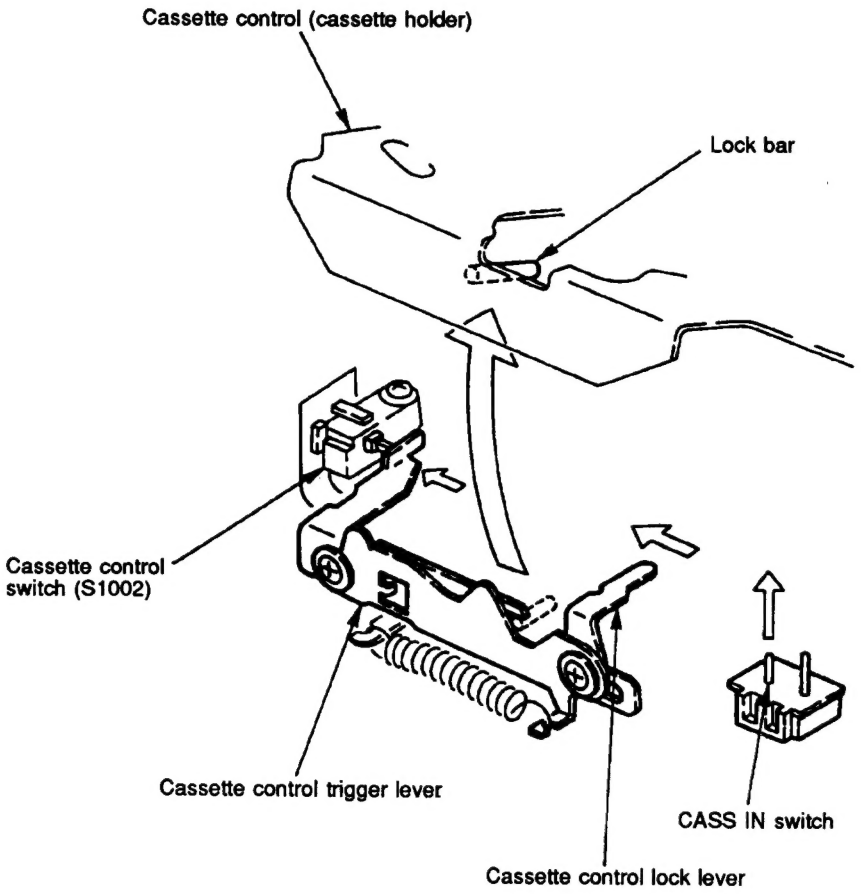

Figure 9-28. Unlocking Cassette Control Lock

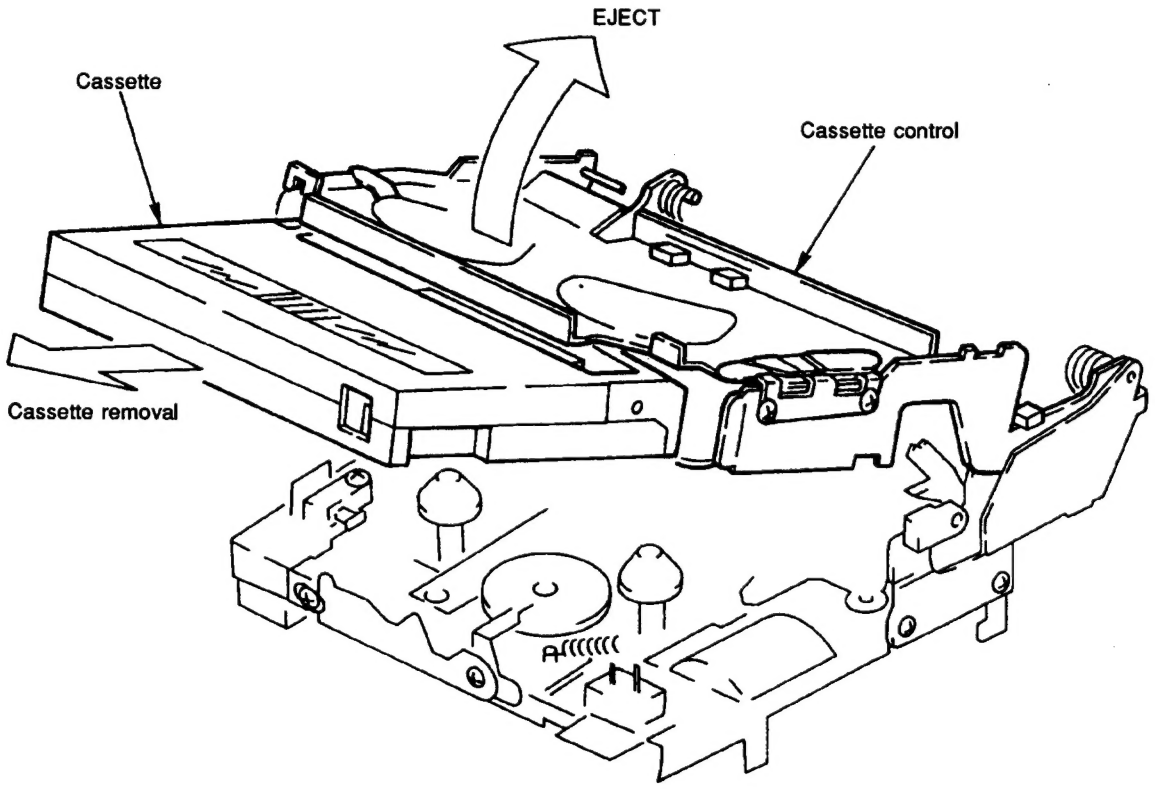

Figure 9-29. EJECT